# MAS6180D

## AM Receiver IC

* **Single Band Receiver IC**
* **High Sensitivity**
* **Very Low Power Consumption**
* **Wide Supply Voltage Range**
* **Power Down Control**
* **Control for AGC On**
* **High Selectivity by Crystal Filter**
* **Fast Startup Feature**

## DESCRIPTION

The MAS6180 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary.

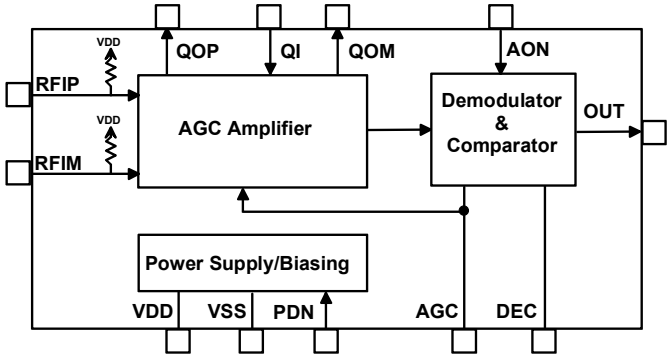
## FEATURES

- Single Band Receiver IC
- Highly Sensitive AM Receiver, 0.4 $\mu V_{RMS}$ typ.
- Wide Supply Voltage Range from 1.1 V to 5.5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Differential Input

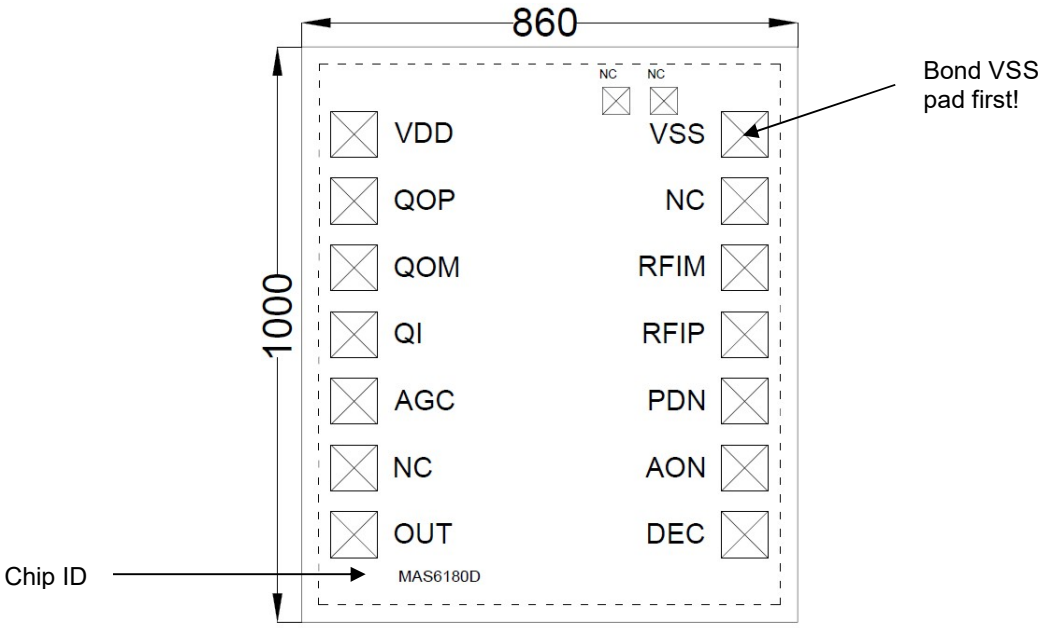
## APPLICATIONS

- Single Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

## BLOCK DIAGRAM



## MAS6180 PAD LAYOUT




DIE size = 860 µm x 1000 µm; PAD size = 80 µm x 80 µm

**Note:** Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

**Note:** Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

| Pad Identification | Name | X-coordinate | Y-coordinate | Note |
|---|---|---|---|---|
| Power Supply Voltage | VDD | 91 µm | 848 µm | |
| Positive Quartz Filter Output | QOP | 91 µm | 732 µm | |
| Negative Quartz Filter Output | QOM | 91 µm | 616 µm | 1 |
| Quartz Filter Input for Crystal | QI | 91 µm | 500 µm | |
| AGC Capacitor | AGC | 91 µm | 384 µm | |
| Not Connected | NC | 91 µm | 268 µm | |
| Receiver Output | OUT | 91 µm | 152 µm | 2 |
| Demodulator Capacitor | DEC | 768 µm | 152 µm | |
| AGC On Control | AON | 768 µm | 268 µm | 3 |
| Power Down | PDN | 768 µm | 384 µm | 4 |
| Positive Receiver Input | RFIP | 768 µm | 500 µm | 5 |
| Negative Receiver Input | RFIM | 768 µm | 616 µm | 5 |
| Not Connected | NC | 768 µm | 732 µm | |
| Power Supply Ground | VSS | 768 µm | 848 µm | |

Notes:
1) QOM bonding pad is not in use in MAS6180D1 version
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
5) Receiver inputs RFIP and RFIM have both 2 MΩ biasing resistors towards VDD

## ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$-$V_{SS}$ | | - 0.3 | +6 | V |
| Input Voltage | $V_{IN}$ | | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| ESD Rating | $V_{HBM}$ | Human Body Model (HBM) (1) | ±2 | | kV |
| | $V_{CDM}$ | Charged Device Model (2) | ±1 | | kV |
| Latchup Current Limit | $I_{LUT}$ | For all pins | ±100 | | mA |
| Operating Temperature | $T_{OP}$ | | -40 | +85 | °C |
| Storage Temperature | $T_{ST}$ | | - 55 | +150 | °C |

Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.
Note 1: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.6V, Temperature = 25°C, unless otherwise specified.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | $T_A$ = -40°C.+85°C | 1.1 | 3.6 | 5.5 | V |
| Current Consumption | $I_{DD}$ | VDD=1.5 V, Vin=0.4 µVrms<br>VDD=3.6 V, Vin=0.4 µVrms<br>VDD=5 V, Vin=0.4 µVrms | | 66<br>68<br>68 | 80<br>85 | µA |
| | | VDD=1.5 V, Vin=20 mVrms<br>VDD=3.6 V, Vin=20 mVrms<br>VDD=5 V, Vin=20 mVrms | | 43<br>42<br>45 | 65<br>65 | µA |
| Stand-By Current | $I_{DDoff}$ | See note below. | | | 0.1 | µA |
| Input Frequency Range | $f_{IN}$ | | 40 | | 100 | kHz |
| Minimum Input Voltage | $V_{IN\ min}$ | | | 0.4 | 1 | µVrms |
| Maximum Input Voltage | $V_{IN\ max}$ | | 20 | | | mVrms |
| Receiver Input Resistance<br>Receiver Input Capacitance | $R_{RFI}$<br>$C_{RFI}$ | Differential Input,<br>f=40 kHz…77.5 kHz | | 700<br>0.6 | | kΩ<br>pF |
| Input Levels $\|I_{IN}\|$<0.5 µA | $V_{IL}$<br>$V_{IH}$ | | <br>$V_{DD}$-0.35 | | 0.35 | V |
| Output Current<br>$V_{OL}$<0.2 $V_{DD}$; $V_{OH}$ >0.8 $V_{DD}$ | $\|I_{OUT}\|$ | | 5 | 15 | | µA |
| DCF77 Output Pulses | $T_{100ms}$<br>$T_{200ms}$ | 1 µVrms ≤ $V_{IN}$ ≤<br>20 mVrms, see note below! | | 95<br>195 | | ms |
| MSF Output Pulses | $T_{100ms}$<br>$T_{200ms}$<br>$T_{300ms}$<br>$T_{500ms}$ | 1 µVrms ≤ $V_{IN}$ ≤<br>20 mVrms, see note below! | | 120<br>220<br>320<br>520 | | ms |
| WWVB Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 1 µVrms ≤ $V_{IN}$ ≤<br>20 mVrms, see note below! | | 200<br>500<br>800 | | ms |
| JJY60 Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 1 µVrms ≤ $V_{IN}$ ≤<br>20 mVrms, see note below! | | 210<br>505<br>800 | | ms |
| JJY40 Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 1 µVrms ≤ $V_{IN}$ ≤<br>20 mVrms, see note below! | | 200<br>495<br>790 | | ms |
| Startup Time | $T_{Start}$ | Fast Start-up, Vin=0.4 µVrms<br>Fast Start-up, Vin=20 mVrms | | 1.3<br>3.5 | 4 | s |
| Output Delay Time | $T_{Delay}$ | | | 50 | 100 | ms |

**Note:** Stand-by current consumption may increase if $V_{IH}$ and $V_{IL}$ differ from VDD and 0 respectively.
**Note:** See Note 6: Time Signal Software's Pulse Width Recognition Limits and Table 5 on page 8!

## TYPICAL APPLICATION

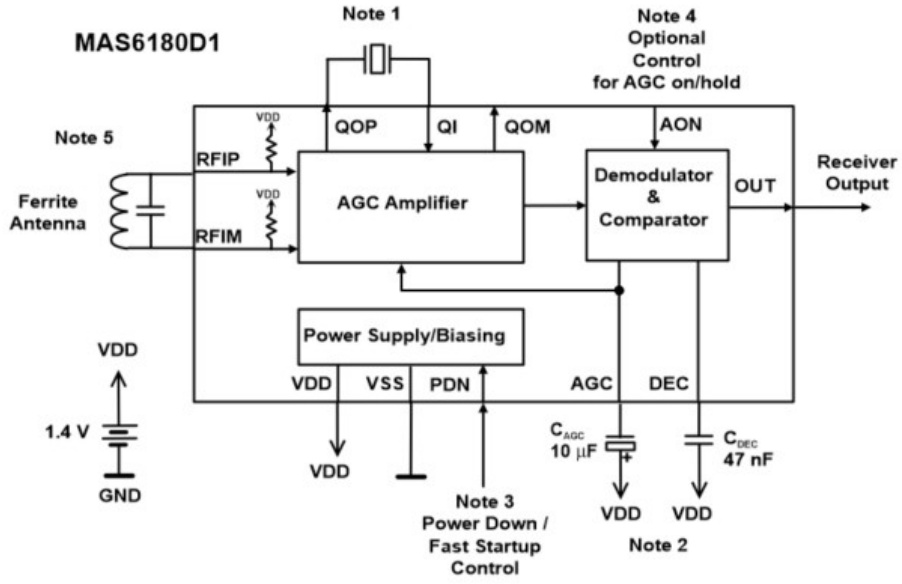



**Figure 1.** Application circuit of internal compensation capacitance option version MAS6180D1.

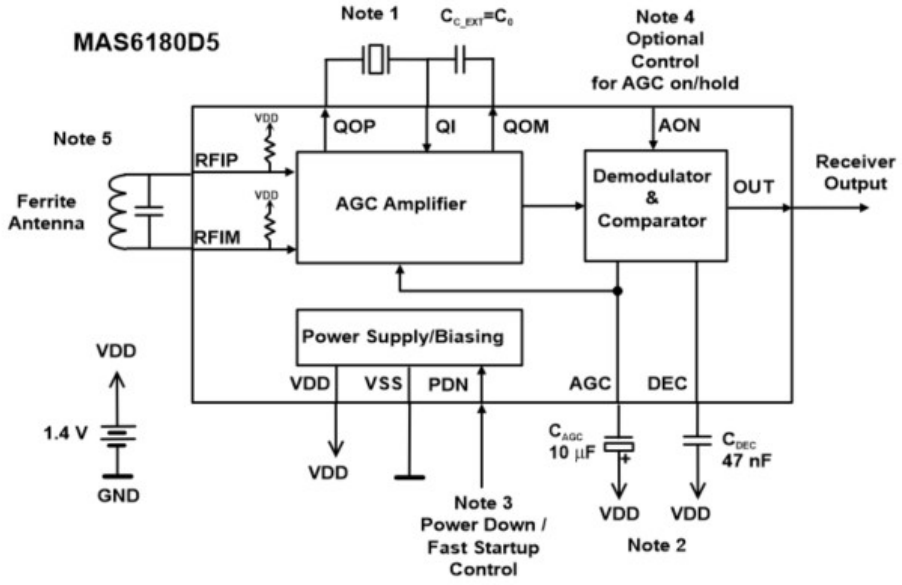



**Figure 2.** Application circuit of external compensation capacitance option version MAS6180D5.

## TYPICAL APPLICATION (Continued)

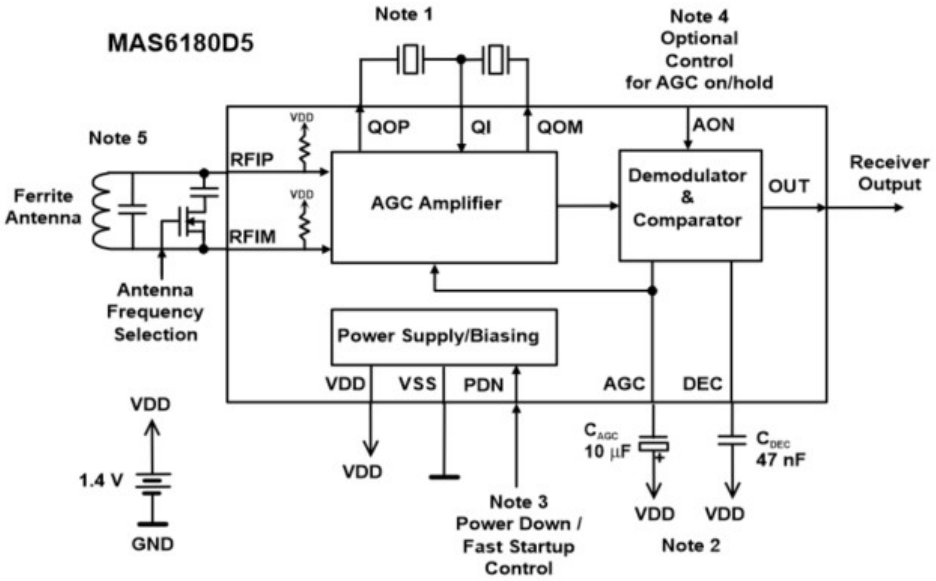



**Figure 3.** Dual band application circuit of external compensation capacitance option version MAS6180D5. PMOS switch transistor is used since RFIM input is biased close to VDD voltage.

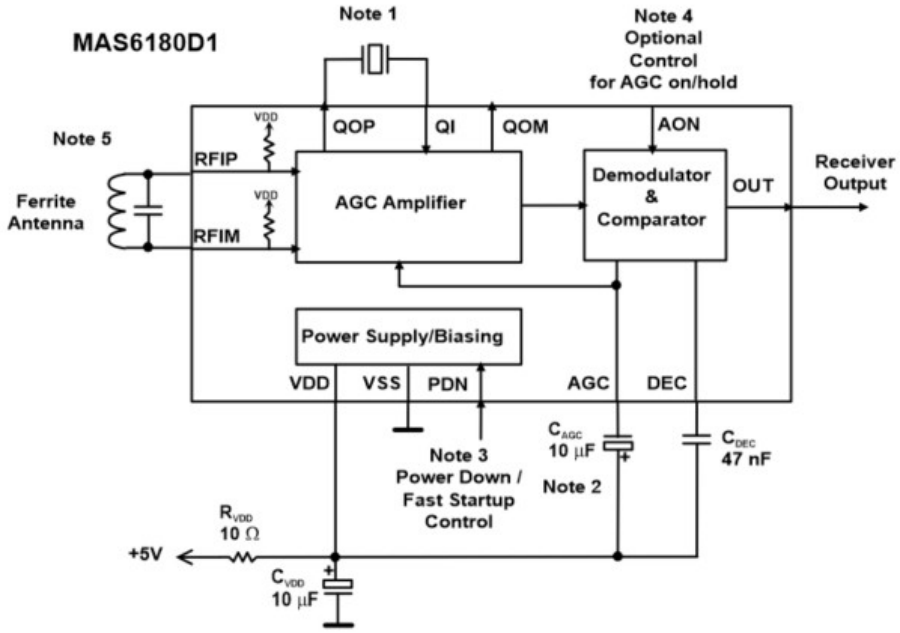



**Figure 4.** Application circuit of internal compensation capacitance option version MAS6180D1 with filtered 5V supply voltage.

## TYPICAL APPLICATION (Continued)

**Note 1: Crystals**
The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). More detailed crystal nominal frequency is normally specified for certain load capacitance but in MAS6180 filter circuit the load capacitance is not used. Effectively this means that most accurate filter frequency is achieved by using about 3 Hz higher frequency crystal than the received time signal frequency. For example, in DCF77 application a 77.503 kHz crystal resonates at the desired DCF77 77.500 kHz frequency when the load capacitor is missing.

**Table 1.** Time-Signal System Frequencies

| Time-Signal System | Location | Antenna Frequency | Recommended Crystal Frequency |
|---|---|---|---|
| DCF77 | Germany | 77.5 kHz | 77.503 kHz |
| HGB | Switzerland | 75 kHz | 75.003 kHz |
| MSF | United Kingdom | 60 kHz | 60.003 kHz |
| WWVB | USA | 60 kHz | 60.003 kHz |
| JJY | Japan | 40 kHz and 60 kHz | 40.003 kHz and 60.003 kHz |
| BPC | China | 68.5 kHz | 68.505 kHz |

The crystal shunt capacitance $C_0$ should be matched as well as possible with the internal shunt capacitance compensation capacitor $C_C$ of MAS6180. MAS6180D5 is option for external crystal compensation capacitor. The external compensation capacitor should be matched similarly as well as possible with crystal's shunt capacitance. See Compensation Capacitance Options on table 2.

**Table 2 .** Compensation Capacitance Options

| Device | $C_C$ | Crystal Description |
|---|---|---|
| MAS6180D1 | 0.75 pF | For low $C_0$ crystals |
| MAS6180D5 | $C_{C\_EXT}$ | For any crystals, external compensation capacitor |

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example, crystal with 1 pF floating package shunt capacitance can have 0.85 pF grounded package shunt capacitance. PCB traces of crystal should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

In dual band receiver configuration, the crystals are best to connect as shown in figure 3. In this configuration the crystals' shunt capacitances compensate each other and external compensation capacitor is not needed at all.

Table 3 below presents some crystal manufacturers having suitable crystals for time signal receiver application.

**Table 3.** Crystal Manufacturers and Crystal Types in Alphabetical Order for Time Signal Receiver Application

| Manufacturer | Crystal Type | Dimensions | Web Link |
|---|---|---|---|
| Citizen | CFV-206 | ø 2.0 x 6.0 | http://www.citizen.co.jp/tokuhan/quartz/ |
| Epson Toyocom | C-2-Type<br>C-4-Type | ø 1.5 x 5.0<br>ø 2.0 x 6.0 | http://www.epsontoyocom.co.jp/english/ |
| KDS Daishinku | DT-261 | ø 2.0 x 6.0 | http://www.kds.info/index_en.htm |
| Microcrystal | MS3V-T1R | 1.45 x 1.45 x 6.7 | http://www.microcrystal.com/ |
| Seiko Instruments | VTC-120 | ø 1.2 x 4.7 | http://www.sii-crystal.com |

## TYPICAL APPLICATION (Continued)

**Note 2: AGC Capacitor**
The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least few 100 MΩ impedance should be used for voltage probing of the AGC and DEC pins. Electrolytic AGC capacitor should have voltage rating at least 25 V for low enough leakage. DEC capacitor can be low leakage chip capacitor.
It is recommended to connect both AGC and DEC capacitors to VDD (see application figure 1) although VSS connection is also possible. The VDD connection provides better supply noise immunity because signals are referenced to VDD. Additionally, leakage currents are minimized in this connection because in power down the AGC pin voltage is pulled to VDD (to minimum AGC gain) then corresponding to zero voltage over the AGC capacitor.

**Note 3: Power Down / Fast Startup Control**
Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered automatically by the falling edge of PDN signal, i.e., controlling device from power down to power up. The VDD must be high before falling edge of PDN to guarantee proper operation of fast startup circuitry. Before power up the device should have been kept in power down state at least 50ms. This guarantees that the AGC capacitor voltage has been completely pulled to VDD during power down. The startup time without proper fast startup control can be over minute but with fast startup it is shortened typically to few seconds.

**Note 4: Optional Control for AGC On/Hold**
AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive of analog clock or watch can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven. The AGC should be in hold only during disturbances and kept on other time released since due to leakage the AGC voltage can change slowly even when in hold.

**Note 5: Ferrite Antenna**
The ferrite antenna converts the transmitted radio wave into a voltage signal. It has an important role in determining receiver performance. Recommended antenna impedance at resonance is around 100 kΩ.
Low antenna impedance corresponds to low noise but often also to small signal amplitude. On the other hand, high antenna impedance corresponds to high noise but also large signal. The optimum performance where signal-to-noise ratio is at maximum is achieved in between.
The antenna should have also some selectivity for rejecting near signal band disturbances. This is determined by the antenna quality factor which should be approximately 100. Much higher quality factor antennas suffer from extensive tuning accuracy requirements and possible tuning drifts by the temperature.

Antenna impedance $R_{ant}$ can be calculated using equation 1 where $f_{res}$, L, $Q_{ant}$ and C are resonance frequency, coil inductance, antenna quality factor and antenna tuning capacitor respectively. Antenna quality factor $Q_{ant}$ is defined by ratio of resonance frequency $f_{res}$ and antenna bandwidth B (equation 2).

$$R_{ant} = 2\pi \cdot f_{res} \cdot L \cdot Q_{ant} = \frac{Q_{ant}}{2\pi \cdot f_{res} \cdot C} = \frac{1}{2\pi \cdot B \cdot C}$$ **Equation 1.**

$$Q_{ant} = \frac{f_{res}}{B}$$ **Equation 2.**

Table 4 on next page presents some antenna manufacturers for time signal application.

## TYPICAL APPLICATION (Continued)

**Table 4.** Antenna Manufacturers and Antenna Types in Alphabetical Order for Time Signal Application

| Manufacturer | Antenna Type | Dimensions | Web Link |
|---|---|---|---|
| Micro Analog Systems Oy | A10X60-77.5K222PY<br>A10X100-77.5K222PY<br>A3.5X4X15-7.87MH<br>A2X3X21-0.92MH<br>A3.75X3.75X23.6-0.92MH | ø 10 x 60 mm<br>ø 10 x 100 mm<br>3.5 x 4 x 15 mm<br>2 x 3 x 21 mm<br>3.75x3.75x23 mm | http://www.mas-oy.com/en/products/radio-controlled-clock-rcc/antennas/ |
| C.E.C Coils | AP/AR Antenna Bars | | http://www.ceccoils.com/CECWEB/index.aspx?lang=en |
| HR Electronic GmbH | 60716 (60 kHz)<br>60708 (77.5 kHz) | ø 10 x 60 mm | http://www.hrelectronic.com/ |
| Hitachi Metals | AN-T702Sxx<br>AN-T702Mxx<br>AN-T702Lxx | 19 x 5.5 x 6.3 mm<br>28 x 5 x 5 mm<br>50 x 5 x 5 mm | http://www.hitachi-metals.co.jp/e/prod/prod06/p06_12.html |
| Premo | RCA-SMD-77A (77.5 kHz)<br>RCA-SMD-60A (60 kHz) | 75 x 15 x 6.3 mm | http://www.grupopremo.com/ |
| Sumida | ACL80A (40 kHz) | ø 10 x 80 mm | www.sumida.co.jp/jeita/XJA021.pdf |

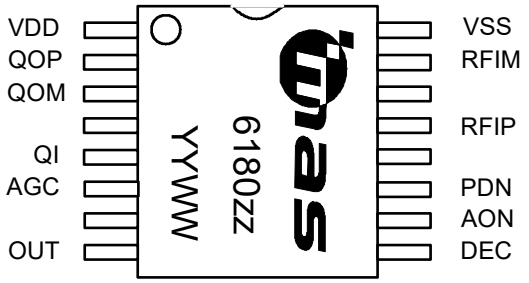
**Note 6: Time Signal Software's Pulse Width Recognition Limits**

The typical output pulse width specifications are presented in the electrical characteristics section on page 3. Due to process variations the typical output pulse width can differ from these. Additionally, the output pulse widths can vary even more depending on the receiving antenna signal strength versus noise and disturbance conditions. That is why it is important that the time signal decoding software has appropriate tolerance limits for managing the output pulse width variations successfully. The table 5 presents recommended software pulse width tolerance limits for recognizing pulses of different time signals.

**Table 5.** Recommended Software Pulse Width Recognition Limits for Different Time Signals

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DCF77 Output Pulses | $T_{100ms}$<br>$T_{200ms}$ | 40<br>140 | 130<br>250 | ms |
| MSF Output Pulses | $T_{100ms}$<br>$T_{200ms}$<br>$T_{300ms}$<br>$T_{500ms}$ | 50<br>170<br>280<br>400 | 160<br>300<br>380<br>600 | ms |
| WWVB Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 100<br>400<br>700 | 300<br>600<br>900 | ms |
| JJY60 Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 100<br>400<br>700 | 300<br>600<br>900 | ms |
| JJY40 Output Pulses | $T_{200ms}$<br>$T_{500ms}$<br>$T_{800ms}$ | 100<br>400<br>700 | 300<br>600<br>900 | ms |

## PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE




Top Marking Definitions:
zz = Version
YYWW = Year Week

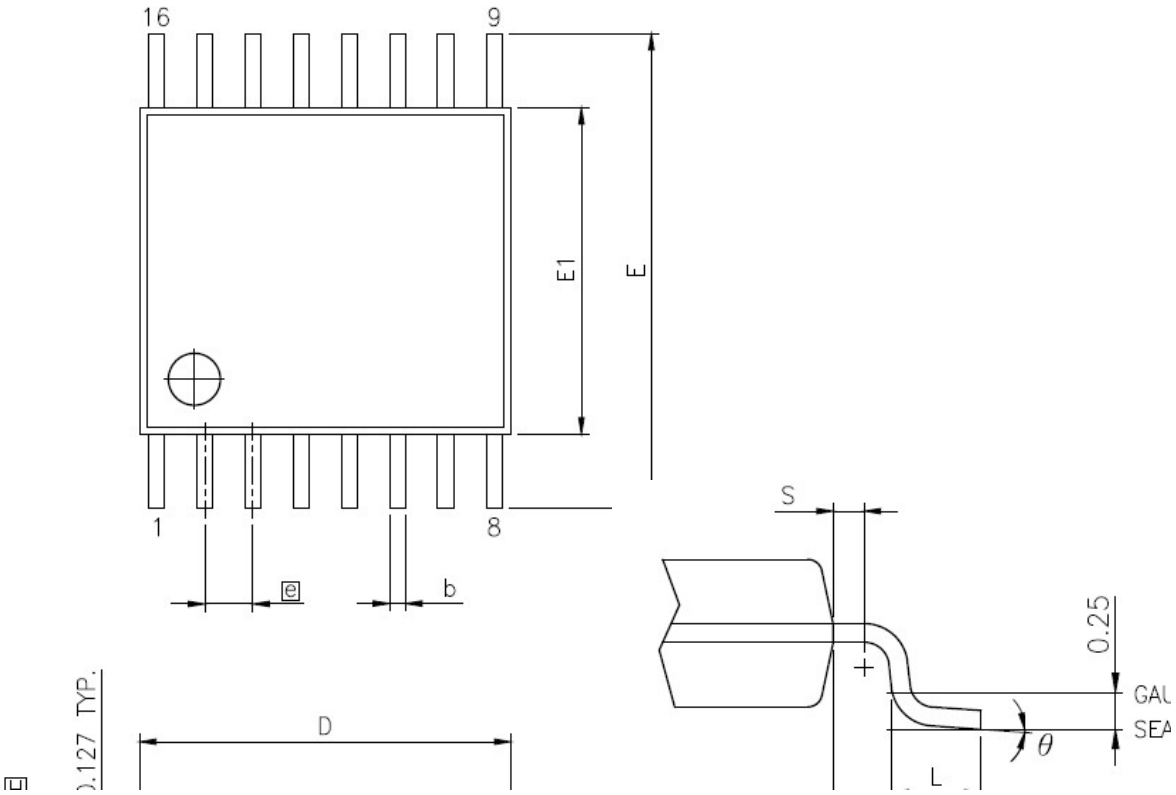
## PIN DESCRIPTION

| Pin Name | Pin | Type | Function | Note |
|---|---|---|---|---|
| VDD | 1 | P | Positive Power Supply | |
| QOP | 2 | AO | Positive Quartz Filter Output | |
| QOM | 3 | AO | Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal | 1 |
| | 4 | NC | | 2 |
| QI | 5 | AI | Quartz Filter Input for Crystal and External Compensation Capacitor | |
| AGC | 6 | AO | AGC Capacitor | |
| | 7 | NC | | 2 |
| OUT | 8 | DO | Receiver Output | 3 |
| DEC | 9 | AO | Demodulator Capacitor | |
| AON | 10 | DI | AGC On Control | 4 |
| PDN | 11 | DI | Power Down Input | 5 |
| | 12 | NC | | 2 |
| RFIP | 13 | AI | Positive Receiver Input | 6 |
| | 14 | NC | | 2 |
| RFIM | 15 | AI | Negative Receiver Input | 6 |
| VSS | 16 | G | Power Supply Ground | |

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:
1) External crystal compensation capacitor pin QOM is connected only in MAS6180D5 version. It is left unconnected in MAS6180D1 version which has internal compensation capacitor.
2) Pin 4 between QOM and QI must be connected to IC's filtered VDD (pin 1) to eliminate TSSOP package lead frame parasitic capacitances disturbing the crystal filter performance and minimizing noise coupling. All other NC (Not Connected) type pins are recommended to be connected to VSS.
3) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
4) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
5) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
6) Receiver inputs RFIP and RFIM have both 2 MΩ biasing resistors towards VDD

## PACKAGE (TSSOP-16) OUTLINES




| Dimension | Min | Nom | Max | Unit |
|---|---|---|---|---|
| A | | | 1.2 | mm |
| A1 | 0.05 | | 0.15 | mm |
| A2 | 0.80 | 1.00 | 1.05 | mm |
| b | 0.19 | | 0.30 | mm |
| D | 4.90 | 5.00 | 5.10 | mm |
| E1 | 4.30 | 4.40 | 4.50 | mm |
| E | | 6.40 BSC | | mm |
| e | | 0.65 BSC | | mm |
| L1 | | 1.00 REF | | mm |
| L | 0.45 | 0.60 | 0.75 | mm |
| S | 0.20 | | | mm |
| θ | 0 | | 8 | ° |

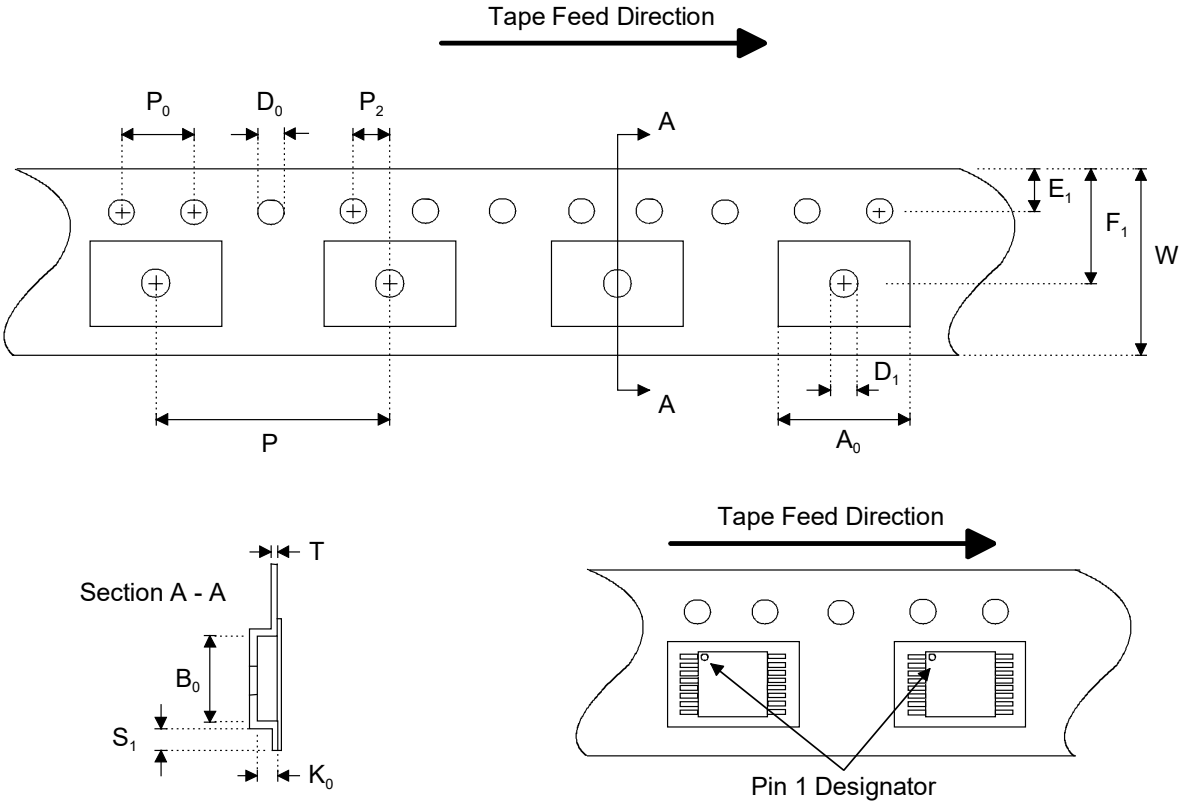
Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

## SOLDERING INFORMATION

◆ **For Pb-Free, RoHS Compliant TSSOP-16**

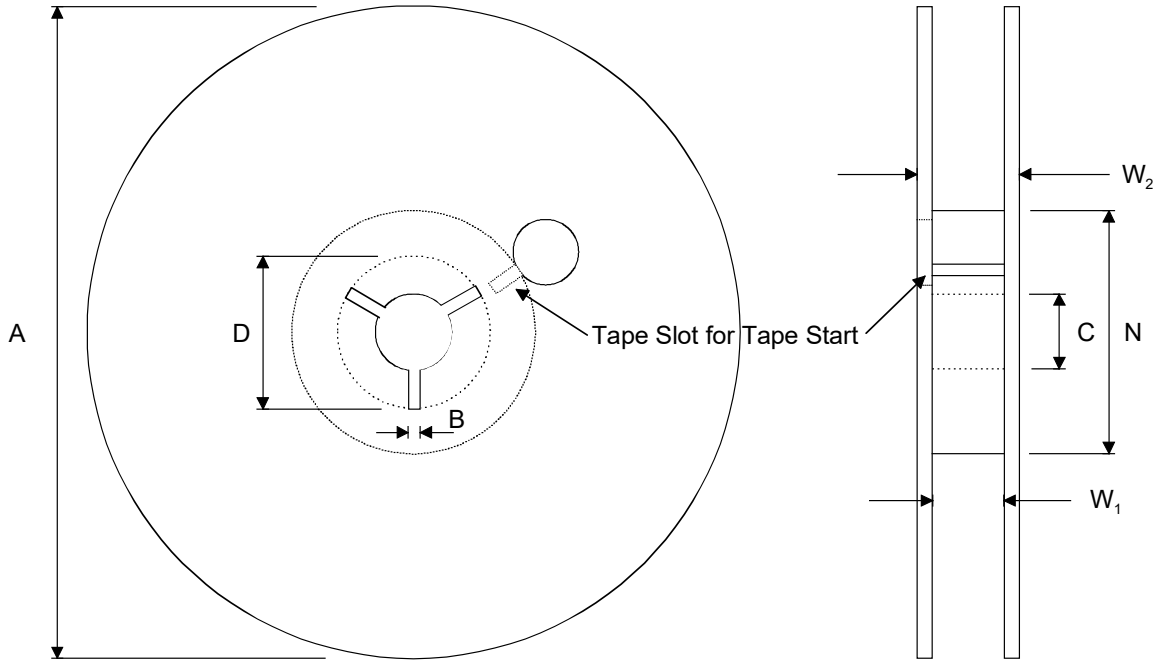
| | |
|---|---|
| Resistance to Soldering Heat | According to RSH test IEC 68-2-58/20 |
| Maximum Temperature | 260°C |
| Maximum Number of Reflow Cycles | 3 |
| Reflow profile | Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org |
| Seating Plane Co-planarity | max 0.08 mm |
| Lead Finish | Solder plate 7.62 - 25.4 µm, material Matte Tin |
| Moisture Sensitivity Level (MSL) | 3 (per J-STD-020) |

## EMBOSSED TAPE SPECIFICATIONS



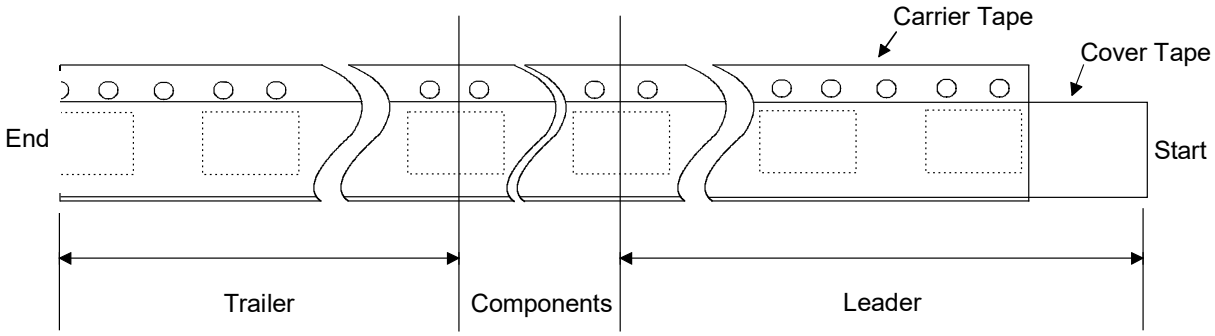

| Dimension | Min | Max | Unit |
|---|---|---|---|
| $A_0$ | 6.50 | 6.70 | mm |
| $B_0$ | 5.20 | 5.40 | mm |
| $D_0$ | 1.50 +0.10 / -0.00 | | mm |
| $D_1$ | 1.50 | | mm |
| $E_1$ | 1.65 | 1.85 | mm |
| $F_1$ | 7.20 | 7.30 | mm |
| $K_0$ | 1.20 | 1.40 | mm |
| P | 11.90 | 12.10 | mm |
| $P_0$ | 4.0 | | mm |
| $P_2$ | 1.95 | 2.05 | mm |
| $S_1$ | 0.6 | | mm |
| T | 0.25 | 0.35 | mm |
| W | 11.70 | 12.30 | mm |

## REEL SPECIFICATIONS




2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative




| Dimension | Min | Max | Unit |
|---|---|---|---|
| A | | 330 | mm |
| B | 1.5 | | mm |
| C | 12.80 | 13.50 | mm |
| D | 20.2 | | mm |
| N | 50 | | mm |
| $W_1$ (measured at hub) | 12.4 | 14.4 | mm |
| $W_2$ (measured at hub) | | 18.4 | mm |
| Trailer | 160 | | mm |
| Leader | 390, of which minimum 160 mm of empty carrier tape sealed with cover tape | | mm |
| Weight | | 1500 | g |

## ORDERING INFORMATION

| Product Code | Product | Description | Capacitance Option |
|---|---|---|---|
| MAS6180D1WA313 | Single Band AM-Receiver IC with Differential Input | EWS-tested non-inked wafer with wafer map, diameter 8”, thickness 406 µm ± 5%. | $C_C$ = 0.75 pF |
| MAS6180D1WA305 | Single Band AM-Receiver IC with Differential Input | EWS-tested dies on tray; thickness 406 µm ± 5%. | $C_C$ = 0.75 pF |
| MAS6180D5WA313 | Single Band AM-Receiver IC with Differential Input | EWS-tested non-inked wafer with wafer map, diameter 8”, thickness 406 µm ± 5%. | External compensation capacitor |
| MAS6180D5WA305 | Single Band AM-Receiver IC with Differential Input | EWS-tested dies on tray; thickness 406 µm ± 5%. | External compensation capacitor |
| MAS6180D1ST208 | Single Band AM-Receiver IC with Differential Input | TSSOP-16, REACH & RoHS compliant, Tube | $_C$ = 0.75 pF |
| MAS6180D1ST206 | Single Band AM-Receiver IC with Differential Input | TSSOP-16, REACH & RoHS compliant, Tape & Reel | $C_C$ = 0.75 pF |

### ◆ The formation of product code

An example for MAS6180D1WA313:

| MAS6180 | D | 1 | WA3 | 00 |
|---|---|---|---|---|
| Product name | Design version | Capacitance option: $C_C$ = 0.75 pF | Package type: WA3 = 406 µm thick EWS tested wafer | Delivery format:<br>05 = dies on tray<br>06 = tape & reel<br>08 = in tube<br>13 = non-inked wafer with wafer map |

## LOCAL DISTRIBUTOR

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