MAS6513

Capacitive Sensor Interface IC

- **Single or Dual Capacitance Sensors**
- **Very Low Power Consumption**
- **On Chip Temperature Sensor**
- **24-Bit Ratiometric ΔΣ CDC**
- **IIR Filter**
- **Built-in 24-Bit Calibration Calculation**
- **512 Bit EEPROM Calibration Memory**
- **Alert Function**
- **SPI and I2C Bus**

DESCRIPTION

MAS6513 capacitive sensor interface IC can interface both single and dual capacitance sensors.

It uses a 24-bit Capacitance-to-Digital Converter (CDC), which employs a delta-sigma (ΔΣ) conversion technique. The output data from the ΔΣ-modulator is processed by an on-chip decimator filter, producing a high resolution conversion result. The converter is run by an internal clock oscillator making an external converter clock unnecessary.

The converter input range is programmable to meet various sensor offset and changing capacitance values. At normal clock frequency maximum sensor capacitance is 20pF but up to 160pF value can be achieved by using available clock division options.

Capacitance resolution is adjustable by capacitance range and over sampling ratio (OSR) configurations.

The MAS6513 supports three different types of capacitance measurements. The output can be proportional either to capacitance difference (C_S-C_R), capacitance ratio (C_S-C_R)/C_S or sum of sensor capacitances (C_S+C_R). The capacitance difference mode offers the highest resolution. The capacitance ratio mode offers pre-linearization for sensors which consist of parallel plates which separation gap depends on measured parameter such as pressure.

The IC is designed especially to meet the requirement for low power consumption, thus making it an ideal choice for battery powered systems. Overall current consumption values down to 0.77 µA (one temperature and capacitance A/D conversion in a second) can be achieved depending on selected resolution setting.

In addition to measuring capacitance the device has an internal temperature sensor for temperature measurement and temperature compensation purposes. The 512-bit EEPROM memory is for storing trimming and calibration coefficients on chip.

Built-in 24-bit DSP block includes IIR filter options and calculation engine which performs calculation of calibrated and temperature compensated sensor and temperature readings. Additional features include alert function and programmable I2C address.

A serial interface, compatible with a bi-directional 2-wire I2C bus and 3-/4-wire SPI bus, is used for conversion setup, starting a conversion and reading the conversion result.

FEATURES

- Sensor Offset and Gain Adjustment
  - Changing Capacitance Range ΔC 1pF…35pF
  - Internal Offset Capacitance Matrix 0pF…22pF
  - External Capacitance up to 160pF
- Noise Resolution down to 29aF
- Internal Clock Oscillator
- On Chip Temperature Sensor -40°C...+125°C
- Wide Operating Voltage Range 1.9V…5.5 V
- Low Average Supply Current: down to 0.77µA typ
- Capacitance conversion Time down to 0.78ms typ
- Internal 512-bit EEPROM Calibration Memory
- Internal Clock Oscillator
- DFN-12 Package

APPLICATIONS

- Humidity Sensors
- Capacitive Pressure Sensors
- Medical Devices
- Flow Meters
- Sport Watches
- Altimeter and Barometer Systems
- Mobile and Battery Powered Systems
- Low Frequency Measurement applications
- Current/Power Consumption Critical Systems
- Industrial and Process Control applications

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BLOCK DIAGRAM

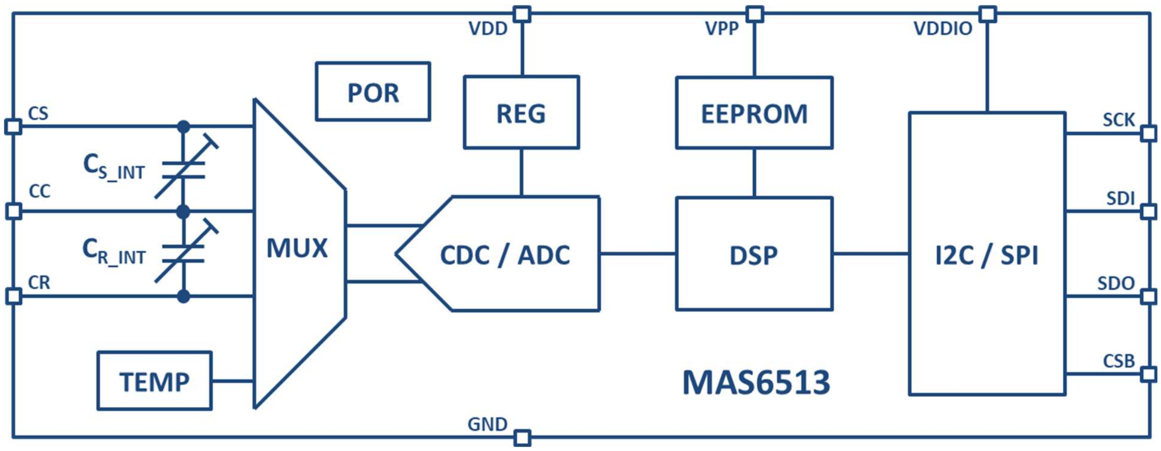


Figure 1. MAS6513 block diagram

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage Pins	V_{DD}, V_{DDIO}		-0.3	7.0	V
Programming Voltage for EEPROM	V_{PP}		-0.3	20	V
Serial Bus Pins		SCK, SDI, SDO, CSB	-0.3	V_{DDIO} + 0.3 or 7V whichever smaller	V
Sensor Pins		CS, CC, CR	-0.3	2.2	V
Latch-Up Current Limit	I_{LU}	For all pins, test according to JESD78E.	-100	+100	mA
Junction Temperature	T_{Jmax}			+ 150	°C
Storage Temperature (1)	T_{STG}		- 55	+125	°C
ESD Rating	V_{HBM} (2)		±2		kV
	V_{CDM} (3)		±1		kV

Note: The absolute maximum rating values are stress ratings only. Functional operation of the device at conditions between maximum operating conditions and absolute maximum ratings is not implied and EEPROM contents may be corrupted. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions above absolute maximum ratings may be destructive to the devices.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).
Note 1: See EEPROM memory data retention at hot temperature. Storage or bake at hot temperatures will reduce wafer level trimming and calibration data retention time.
Note 2: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 3: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		1.9	3.3	5.5	V
Serial Bus Supply Voltage	V_{DDIO}		1.2	3.3	5.5	V
Programming Voltage for EEPROM (1)	V_{PP}		16.5	17.0	17.5	V
Operating Temperature	T_A		-40	+25	+125	°C

Note 1: EEPROM programming voltage is needed only in EEPROM write. In read only applications the VPP pin should be grounded. EEPROM write operation is possible over operating temperature range but it is recommended to be done at room temperature.

ELECTRICAL CHARACTERISTICS

Operating Conditions: T_A = -40°C to +125°C, Typ VDD = VDDIO = 3.3V, Typ T_A = 27°C, DIV=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal regulator voltage	V_{REG}		1.62	1.8	1.9	V
Sleep current (1)	I_{SLEEP}	T_A = 27°C T_A = 125°C		0.09 1.2	0.2 4	µA
Standby current (1)	I_{STDBY}	Internal clock External clock		21 13	38 30	µA
Conversion current consumption (2)	I_{DD_DIFF} I_{DD_RATIO} I_{DD_SUM} I_{DD_TEMP}	Difference mode capacitance Ratio mode capacitance Sum mode capacitance Temperature	430 380 430 280	730 640 730 510	1060 980 1060 810	µA
Internal clock oscillator frequency (3)	f_{OSC}	VDD = 3.3V, T_A = 27°C Over full VDD and temp range	1.92 1.5	2.0 2.0	2.08 2.5	MHz
Temperature conversion clock frequency (4)	f_{CLK_TEMP}	Over VDD and temp range	187	250	313	kHz
Capacitance conversion clock frequency (4)	f_{CLK_CAP}	Over VDD and temp range Normal system clock (DIV=00) Division by 2 (DIV=01) Division by 4 (DIV=10) Division by 8 (DIV=11)	 93.75 46.875 23.437 11.718	 125 62.5 31.25 15.625	 156.25 78.125 39.063 19.532	kHz
Conversion time (4)	t_{CAP}	Normal system clock (DIV=00) OSR=1x OSR=2x OSR=4x OSR=8x OSR=16x OSR=32x OSR=64x	 0.63 1.04 1.86 3.49 6.77 13.32 26.43	 0.78 1.30 2.32 4.37 8.46 16.66 33.04	 1.05 1.73 3.09 5.82 11.29 22.21 44.05	ms
	t_{TEMP}	OSR=1x OSR=2x OSR=4x OSR=8x OSR=16x OSR=32x OSR=64x	0.31 0.52 0.93 1.75 3.39 6.66 13.22	0.39 0.65 1.16 2.18 4.23 8.33 16.52	0.52 0.86 1.55 2.91 5.64 11.10 22.03	ms
Calculation time (5)	t_{CALCT}	Calculation enabled	0.048	0.05	0.052	ms
	t_{CALCC}	(XCALC=0)	0.202	0.21	0.219	ms

Note 1. All inputs at VDDIO, no load. Leakage current may increase if digital input voltages are not close to VDDIO (high) or GND (low).
Note 2. Conversion current consumption values are measured using following settings; CMM=00, OCDACS=OCDACR=55$_{HEX}$ (C_{S_INT} = C_{R_INT} = 7.33pF), GRDAC=55$_{HEX}$ (ΔC=6.22 pF). Average current consumption is typically much less than this since conversion time is typically very short when compared to measurement repetition period. See table 2 for average current consumption values.
Note 3. The clock oscillator is factory calibrated. Calibration stored in the Oscillator frequency trim data EEPROM address (3F$_{HEX}$).
Note 4. There are four system clock division (DIV) options available; division by 1 (non-divided), 2, 4 and 8. Division options have effect on capacitance measurements only. Temperature measurements are always run using non-divided system clock independent of the DIV selection. In case of capacitance measurement, the conversion times presented here will be multiplied by the selected division factor.
Note 5. Calibrated temperature and capacitance calculations are performed after A/D conversion only if calculations are enabled (XCALC=0).

ELECTRICAL CHARACTERISTICS

Operating Conditions: T_A = -40ºC to +125ºC, Typ VDD = VDDIO = 3.3V, Typ T_A = 27ºC, DIV=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal offset capacitor matrix selection	C_{R_INT} C_{S_INT} C_{INT_STEP}	$OCDACS=255_{DEC}$ $OCDACR=255_{DEC}$	18.7 18.7	22 22 0.0863	25.3 25.3	pF
Linear input capacitance range of changing sensor capacitance in capacitance difference and sum modes (1)	ΔC_{DIFF} (4)	CMM=00 Normal clock (DIV=00) Division by 2 (DIV=01) Division by 4 (DIV=10) Division by 8 (DIV=11)	 2 2 2 2		 20 35 35 35	pF
		CMM=01 Normal clock (DIV=00) Division by 2 (DIV=01) Division by 4 (DIV=10) Division by 8 (DIV=11)	 1 1 1 1		 17 17 17 17	pF
	ΔC_{SUM} (4)	CMM=11 Normal clock (DIV=00) Division by 2 (DIV=01) Division by 4 (DIV=10) Division by 8 (DIV=11)	 2 2 2 2		 20 30 30 30	pF
Maximum allowed sensor capacitance in capacitance difference mode (1)	$C_{S\_MAX\_DIFF}$ (4)	CMM=00 Normal clock (DIV=00) Division by 2 (DIV=01) Division by 4 (DIV=10) Division by 8 (DIV=11)			 20 40 80 160	pF
Linear input capacitance range of changing sensor capacitance in capacitance ratio mode (2)	ΔC_{RATIO} (4)	CMM=10	2		20	pF
Maximum allowed sensor capacitance in capacitance ratio mode (2)	$C_{S\_MAX\_RATIO}$ (4)				20	pF
Internal PTAT temperature sensor (3)	Linearity			±0.3		°C
	Slope			43000		LSB/ °C
		Non-calibrated T_A = 27°C	-6		4	%
	Offset	Non-calibrated T_A = 27°C	-10		10	°C
Temperature resolution	T_N	OSRT=1x OSRT=2x OSRT=4x OSRT=8x OSRT=16x OSRT=32x OSRT=64x		0.045 0.030 0.020 0.016 0.012 0.009 0.008		$°C_{RMS}$

Note 1. In capacitance difference mode the maximum allowed sensor and reference capacitor values can be extended using lower system clock frequencies which are available via system clock divider (DIV) options; C_{S_MAX} = 20pF*125kHz / f_{CLK_CAP}.
Note 2. In capacitance ratio mode, also larger capacitances are possible depending on sensor characteristics. Please contact Micro Analog Systems to check sensor suitability.
Note 3. Linearity from best fit straight line. Guaranteed by design. By first order calibration of offset and slope an overall temperature accuracy close to the linearity accuracy can be achieved. Further accuracy can be achieved by second order calibration to reduce non-linearity errors. Minimum and maximum values of temperature sensor gain and offset are guaranteed by design.
Note 4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS

Operating Conditions: T_A = -40ºC to +125ºC, Typ VDD = VDDIO = 3.3V, Typ T_A = 27ºC, DIV=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EEPROM size				512		bit
EEPROM data write time (1)	t_{WRITE}		17	22	30	ms
EEPROM data retention (2)		T_A = +125 °C	10			years
Full scale output code range	CODEFS		0		11184810	count
Linear output code range values (10%...90% of CODEFS)	CODELIN		1118481		10066329	count
VDD sensitivity of capacitance measurement (3)	VDDSENSD	Difference mode CMM=00, ΔC_{LIN}=4pF, CS=CR=8pF VDD=2V ⇒ 5.5V		0.002		%FS/V
	VDDSENSR	Ratio mode CMM=10, ΔC_{LIN}=4pF, CS=4.3pF, CR=5.7pF VDD=2V ⇒ 5.5V		0.0033		%FS/V
VDD sensitivity of temperature measurement (3)	VDDSENST	VDD=2V ⇒ 5.5V		0.003		%FS/V

Note 1. There should be at least a 30 ms delay after each EEPROM write since EEPROM programming can take up to 30 ms.
Note 2. Data retention values apply when extended EEPROM tests are done. Please contact Micro Analog Systems Oy if the data retention values here need to be guaranteed by comprehensive EEPROM testing.
Note 3. VDD sensitivity in %FS/V calculated as follows: VDD_{SENS} =100%*((CODE @ VDD_{MAX}) – (CODE @ VDD_{MIN}))/CODEFS/(VDD_{MAX} - VDD_{MIN}) where VDD_{MAX}=5.5V and VDD_{MIN}=2V. Difference mode setup: OCDACS,R=93_{DEC}, GRDAC=109_{DEC} , Ratio mode setup: OCDACS=50_{DEC}, OCDACR=66_{DEC}, GRDAC=92_{DEC}

♦ Digital inputs

T_A = -40ºC to +125ºC, VDD = 1.9V to 5.5V, Typ T_A = 27ºC, Typ VDD = VDDIO = 3.3 V, R_P = 4.7kΩ I2C bus pull up, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Serial Bus Clock Frequency	f_{SCK}	I2C bus SPI bus			400 2	kHz MHz
Wait time after power-up (1)	t_{PUP_WAIT}		300			µs
Input High Voltage	V_{IH}		80% VDDIO		100% VDDIO	V
Input Low Voltage	V_{IL}		0% VDDIO		20% VDDIO	V
Input High Voltage	I_{IH}	CSB, SCK, SDI		0.01	0.2	µA
Input Low Voltage	I_{IL}	SCK, SDI	-0.2	-0.01		µA
CSB Pin Pull Up Current (2)	I_{IL_CSB}	CSB=0V	-40	-12	-1	µA

Note 1. This is the necessary wait time after power-up to make sure that power-on reset (POR) circuit has released the device from a reset
Note 2. CSB pin pull up current is disabled in Test modes

♦ Digital outputs

T_A = -40ºC to +125ºC, VDD = 1.9V to 5.5V, Typ T_A = 27ºC, Typ VDD = VDDIO = 3.3 V, R_P = 4.7kΩ I2C bus pull up, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output high voltage	V_{OH}	I_{Source}=0.6mA	80% VDDIO		100% VDDIO	V
Output low voltage	V_{OL}	I_{Sink}=0.6mA	0% VDDIO		20% VDDIO	V
Signal rise time (from 10% to 90%)	t_r	SDO pin, C_L=50pF I2C: SDI pin, C_B=50pF		3.5 530		ns
Signal fall time (from 90% to 10%)	t_f	SDO pin, C_L=50pF SDI pin, C_B=50pF		3.4 3.4		ns

ELECTRICAL CHARACTERISTICS

Table 1. Typical A/D conversion and calibration calculation durations

OSRT [-]	OSRC [-]	t_{TEMP} [ms]	t_{CAP} [ms]	t_{CALC_T} [ms]	t_{CALC_C} [ms]	t_{TOTAL} [ms]	Max f_{RATE} [Hz]
1x	1x	0.39	0.78	0.05	0.21	1.46	684
2x	2x	0.65	1.30	0.05	0.21	2.23	448
4x	4x	1.16	2.32	0.05	0.21	3.76	265
4x	8x	1.16	4.37	0.05	0.21	5.81	172
4x	16x	1.16	8.46	0.05	0.21	9.91	100
4x	32x	1.16	16.66	0.05	0.21	18.10	55
8x	64x	2.18	33.04	0.05	0.21	35.51	28

Note: Above typical time values are subject to ±25% variations due to internal clock oscillator frequency dependency on VDD and temperature

Table 2. Average current consumption in temperature and capacitance difference modes

OSRT [-]	OSRC [-]	IDD_{AVE_TEMP} [µA]	IDD_{AVE_CAP} [µA]	IDD_{AVE_TOT} [µA]
1x	1x	0.20	0.57	0.77
2x	2x	0.33	0.95	1.28
4x	4x	0.59	1.70	2.29
4x	8x	0.59	3.19	3.79
4x	16x	0.59	6.18	6.78
4x	32x	0.59	12.16	12.76
8x	64x	1.12	24.12	25.24

Note: Average current consumption in one shot mode at measurement rate of 1Hz and when capacitance difference mode (CMM=00) is selected and calibration calculation is enabled (XCALC=0).

Table 3. Typical RMS noise resolution in capacitance difference mode with standard input range (CMM=00)

OSRC [-]	C_N [aF$_{RMS}$] @ ΔC_{LIN}=2pF CMM=00 OCDACS,R=00$_{DEC}$ GRDAC=229$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=2pF CMM=00 OCDACS,R=81$_{DEC}$ GRDAC=229$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=4pF CMM=00 OCDACS,R=93$_{DEC}$ GRDAC=109$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=8pF CMM=00 OCDACS,R=185$_{DEC}$ GRDAC=49$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=20pF CMM=00 OCDACS,R=232$_{DEC}$ GRDAC=13$_{DEC}$
1x	350	690	1100	3800	11000
2x	200	400	760	2500	7100
4x	130	260	540	1800	5000
8x	95	180	420	1200	3700
16x	64	130	280	870	2500
32x	49	91	210	610	1800
64x	37	68	140	450	1300

Note: Capacitive sensor emulated by using on-chip offset capacitor matrices. Noise values at mid code range output code value.

Table 4. Typical RMS noise resolution in capacitance difference mode with narrow input range (CMM=01)

OSRC [-]	C_N [aF$_{RMS}$] @ ΔC_{LIN}=1pF CMM=01 OCDACS,R=00$_{DEC}$ GRDAC=229$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=1pF CMM=01 OCDACS,R=41$_{DEC}$ GRDAC=229$_{DEC}$
1x	150	360
2x	140	240
4x	110	170
8x	78	120
16x	55	86
32x	41	63
64x	29	45

Note: Capacitive sensor emulated by using on-chip offset capacitor matrices. Noise values at mid code range output code value.

Table 5. Typical RMS noise resolution in capacitance ratio mode

OSRC [-]	C_N [aF$_{RMS}$] @ ΔC_{LIN}=2pF, CMM=10 OCDACS=79$_{DEC}$ OCDACR=67$_{DEC}$ GRDAC=59$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=4pF, CMM=10 OCDACS=87$_{DEC}$ OCDACR=66$_{DEC}$ GRDAC=92$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=8pF, CMM=10 OCDACS=132$_{DEC}$ OCDACR=92$_{DEC}$ GRDAC=173$_{DEC}$	C_N [aF$_{RMS}$] @ ΔC_{LIN}=20pF, CMM=10 OCDACS=174$_{DEC}$ OCDACR=107$_{DEC}$ GRDAC=149$_{DEC}$
1x	1400	1800	2500	3100
2x	1200	1400	1800	2000
4x	1000	960	1300	1400
8x	810	770	920	950
16x	600	570	650	740
32x	420	400	470	490
64x	310	280	340	350

Note: Capacitive sensor emulated by using on-chip offset capacitor matrices. Noise values at mid code range output code value.

FUNCTIONAL DESCRIPTION

♦ Power on reset

The MAS6513 has power on reset (POR) circuitry which resets the device into sleep mode after both power supplies VDD and VDDIO have risen to sufficient levels. The VDD is supply voltage for analog and digital blocks and the VDDIO is supply voltage for the digital I2C and SPI serial bus interface. There are no limitations for the slope and sequence of raising of the VDD and VDDIO supplies. However, it is recommended to reset the device manually after every power up to make sure it is reset properly. This is accomplished by writing B4$_{HEX}$ (1011 0100$_{BIN}$) to the Reset register address 40$_{HEX}$ via the I2C or SPI serial bus interface.

Reset initializes internal counters, serial communication bus and all registers from 40$_{HEX}$ to 7F$_{HEX}$ to default values. See table 7 for MAS6513 register map and reset values.

♦ Digital interface selection

The MAS6513 supports I2C and SPI digital interfaces. The I2C interface is a 2-wire serial bus which is selected by leaving the CSB pin unconnected (floating) or by connecting it to VDDIO. The CSB pin has internal 250 kΩ pull-up resistor to VDDIO. Note: The 2-wire I2C bus of MAS6513 supports basic I2C bus communication protocol but not 10-bit addressing and clock stretching features of the I2C bus specification.

The SPI interface supports 3-wire and 4- wire serial bus communication. Selection between 3- and 4-wire SPI bus modes is done by SDOFS bits in the Configuration register 1 (41$_{HEX}$). See table 8 on page 20. After power up the SDOFS=00 which selects the 4-wire SPI bus mode. To select 3-wire SPI bus mode it is necessary to first set SDOFS=01 in the Configuration register 1.

The SPI communication is selected by pulling the CSB pin low. It has an additional SPI mode lock in feature. By pulling CSB low and giving at least four SCK clock pulses makes the digital interface to lock into SPI communication mode. This is done in order to avoid inadvertently decoding SPI traffic as another slave device I2C data. After entering SPI lock mode, the I2C communication is possible only after applying power on reset (switching power supply off and on).

♦ Temperature sensing

MAS6513 has on-chip temperature sensor for temperature sensing. The temperature sensor output is proportional to absolute temperature (PTAT). The temperature information is needed for both temperature indication and temperature compensation. For further details see chapter TEMPERATURE MEASUREMENT.

♦ Capacitance sensing

MAS6513 supports three different capacitance measurement modes. The output can be proportional either to capacitance difference (C_S-C_R), capacitance ratio (C_S-C_R)/C_S or sum of capacitances (C_S+C_R). The capacitance difference mode has the highest resolution and the capacitance ratio mode offers pre-linearization for sensors which consist of parallel plates. One example of such type of sensor is pressure sensor in which separation gap of electrode plates depends on pressure.

MAS6513 can interface both single and dual capacitance sensors. Single capacitance sensors should be connected between CS and CC inputs. The second capacitor of a dual capacitance sensor should be connected between CR and CC inputs. The MAS6513 has two internal up to 22pF capacitor matrices for sensor offset adjustment. Changing input capacitance range is adjusted by gain register. For further details see chapter CAPACITANCE MEASUREMENT MODES on pages 38-40 and tables 19-21 on page 29 for capacitive front-end trimming registers.

♦ Operating modes

Only three registers are needed to configure and run on-chip temperature sensor and external capacitive sensor measurements. Configuration register 1 (41_{HEX}) and Configuration register 2 (42_{HEX}) contain only measurement configuration settings. See Configuration register description tables 8-9 on pages 18-19. The Control register (43_{HEX}) contains measurement resolution and operating mode selection settings. Writing to Control register starts the selected measurements. See table 10 on page 22.

MAS6513 has three operating modes; 1) sleep mode, 2) one shot mode and 3) continuous mode. The operating mode is selected by MODE bits in the Control register. Operating modes and their selection are illustrated in the figure 2.

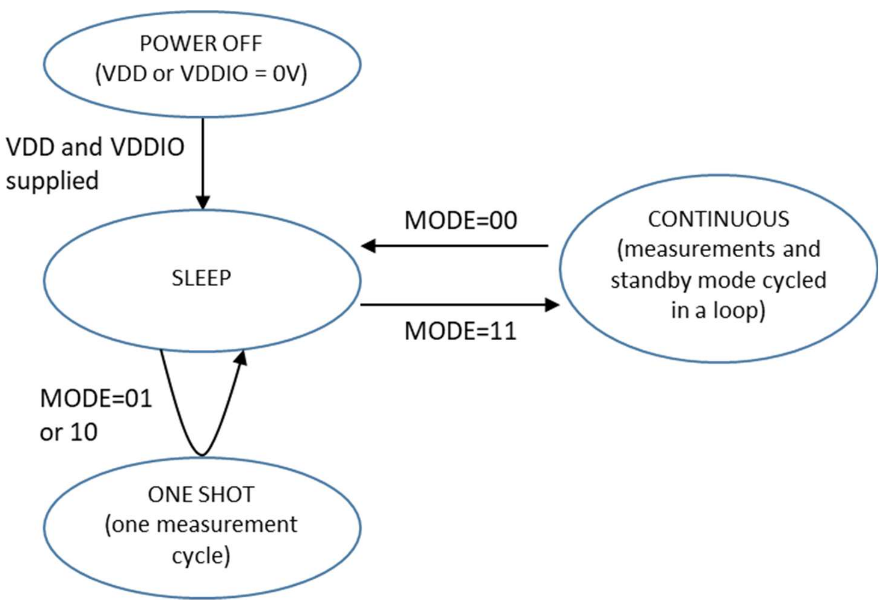


Figure 2. Operating modes and their selection

After power up (both VDD and VDDIO supplied) internal power-on-reset (POR) circuit resets the device and sets it into the sleep mode (MODE=00). In the sleep mode the device does not perform any action and only a very low leakage current is drawn from the supplies.

By setting MODE=01 or 10 makes the device to enter one shot mode in which selected measurements are run only once after which the device returns automatically to the sleep mode. Every new measurement requires writing a new one shot mode command (MODE=01 or 10) into the Control register. In the one shot mode an internal clock oscillator is turned on only during the measurement. The one shot mode is recommended in applications that use low measurement rate or require host based synchronization of measurements.

Important note: After giving one shot (MODE=01 or 10) or continuous (MODE=11) mode command there should be at least 55µs delay between end of the command and before reading data from or writing data to the MAS6513. This is because after every start command the MAS6513 reserves internal data bus for up to 55µs during which trimming data and calibration coefficients are transferred from EEPROM to corresponding registers. Any data read from or written to the MAS6513 is not valid during this time period.

In one shot mode MAS6513 performs at first temperature measurement but only if setting OSRT<>000 has been chosen in the Control register. This is followed by capacitance measurement but only if it has been chosen by setting OSRC<>000. After measurements there is calculated calibrated temperature and temperature compensated capacitance readings but only if the calculation has been enabled (XCALC=0) in the Configuration register 1.

The resulted 24-bit temperature and capacitance readings are stored to the temperature ($45…47_{HEX}$) and capacitance ($48…4A_{HEX}$) result registers after which the device enters the sleep mode. See figure 3 illustrating one shot mode timing and current consumption. Note that the IDD levels and time scale in figures 3 and 4 are not in correct proportion but illustrative only.

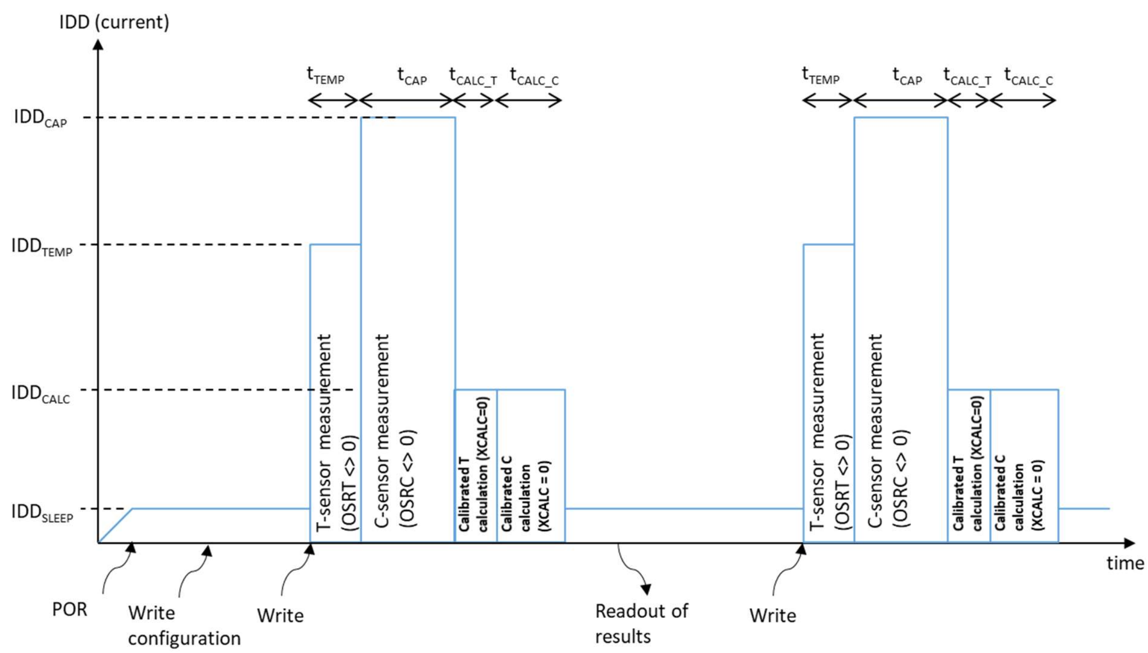


Figure 3. One shot mode timing and current consumption

Selection of temperature and capacitance measurement and their resolution is done independently using eight different OSRT and OSRC over sampling ratio (OSR) settings. Smaller OSR setting corresponds to lower resolution but also to shorter measurement time and lower average current consumption. Similarly, larger OSR setting means higher resolution but longer measurement time and higher average current consumption. The available eight different OSR settings give large flexibility to make optimization between resolution, measurement data rate and average current consumption. See further performance details in ELECTRICAL CHARACTERISTICS on pages 3-6.

By setting MODE=11 makes MAS6513 to enter continuous mode. It is recommended in applications where IIR filter is used like to filter short-term sensor signal disturbances. In continuous mode measurements selected by the OSRT and OSRC settings are repeated in a loop until sleep mode (MODE=00) is selected. Similarly, to one shot mode also calibration calculations are performed but only when enabled (XCALC=0). Between repeated measurements the device enters standby mode. To save power only internal clock oscillator is running during the standby mode. Length of the standby mode (t_{DELAY}) is selectable from 0ms (no delay) up to 2048ms by using DELAY bits in the Configuration register 2. See table 9 on page 21. See figure 4 illustrating continuous mode timing and current consumption.

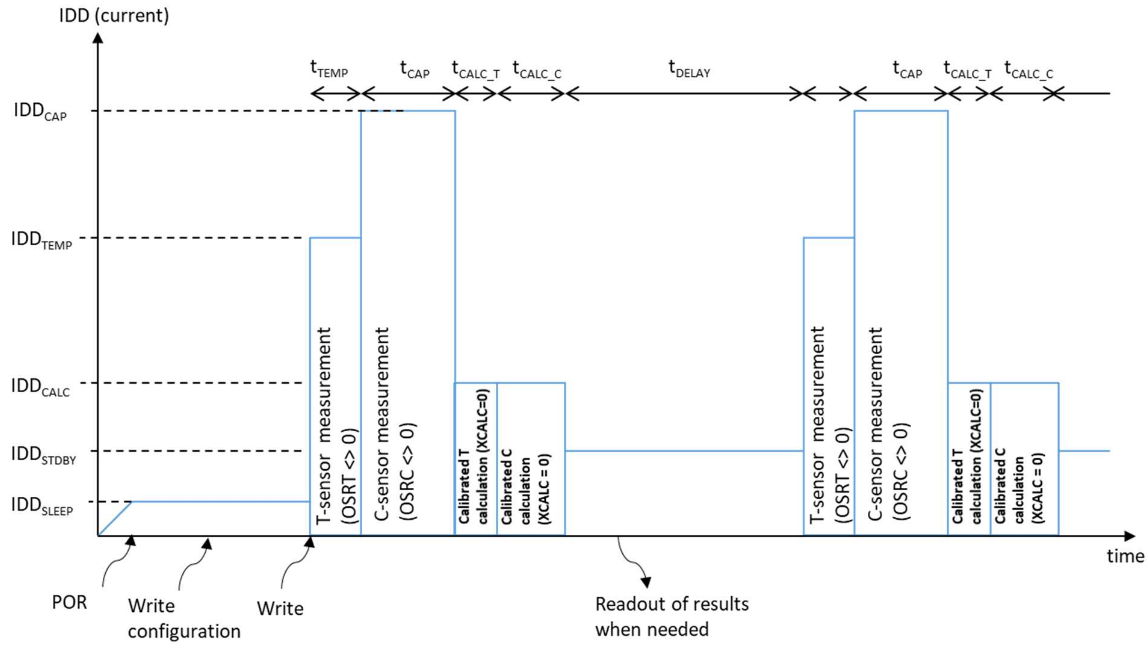


Figure 4. Continuous mode timing and current consumption

♦ Digital IIR low pass filter

The Configuration register 2 (42_{HEX}) has selection for a digital infinite impulse response (IIR) type low pass filter with no filtering and seven different filtering options. See table 9 on page 21. The IIR low pass filter can be used to damp sudden variations in the sensor signal and to further improve noise resolution by an additional filtering of the noise. The filter does not affect output data rate but step response delay and band-width of the output signal. When selected the filtering is applied to both temperature and capacitance signals. The IIR filter works in both single shot and continuous modes. Changing FILTER setting from 000 value to <> 000 value initializes the filter.

See also IIR filter step response and noise filtering information in chapter APPLICATION INFORMATION on page 48.

♦ Reading measurement results

MAS6513 temperature and capacitance measurement results are 24-bit unsigned numbers each of which are stored into three 8-bit result registers. The temperature result register addresses are MSB byte (45_{HEX}), LSB byte (46_{HEX}) and XLSB byte (47_{HEX}). The capacitance result register addresses are MSB byte (48_{HEX}), LSB byte (49_{HEX}) and XLSB byte ($4A_{HEX}$).

Depending on FILTER setting the results can be raw (FILTER=000) or filtered (FILTER<>000) ADC results. Additionally, depending on XCALC setting the results can be non-calibrated (XCALC=1) or calibrated (XCALC=0) measurement results. See tables 12-13 on page 24 for details.

The MAS6513 measurement status and result availability can be monitored using Status register (44_{HEX}) which contains RDYx flags to indicate when there are unread temperature (x=T) and/or capacitance (x=C) measurement results available in the temperature and capacitance result registers. Depending on XCALC setting the RDYx flags are set (1) after corresponding measurement (XCALC=1) or after calibration calculation (XCALC=0) has been finished and new result is ready and available for reading. Reading temperature (x=T) or/and capacitance (x=C) result from the result registers will clear (0) the corresponding RDYx flag.

The decision when to read measurement results can be based on by three different methods; 1) Using interrupts, 2) Polling Status register or 3) Waiting maximum time which can take a new result to come available.

The interrupts can be enabled to SDO pin by using SDOFS and INTSEL bit settings in the Configuration register 1. See table 8 on page 20.

The Status register has RDYT and RDYC flags which are set high when new calibrated value or A/D conversion result is ready for reading. Thus, polling state of these flags in the Status register tells when results are available for reading. See table 11 on page 23 for further details.

The third method is to wait maximum time that can take to finish selected measurements and calculations and in case of continuous mode after additional standby delay time which has been selected before reading the results.

See figure 5 for Calibrated MAS6513 sensor system measurement flow. In continuous mode it is also possible to read results at a rate when new results are expected to be ready. This is possible since MAS6513 has internal A/D conversion result memory buffer. If new result is finished during read of result registers the new value is updated result registers only after the serial bus communication has been released. **Important note: In continuous mode the results must be always read using burst read** (all three bytes of each result or all six bytes of both results in a single read sequence) to maintain data consistency. See table 26 example of the burst read by 2-wire serial data interface (I2C bus) protocol. The burst read is recommended to be used also in the one shot mode.

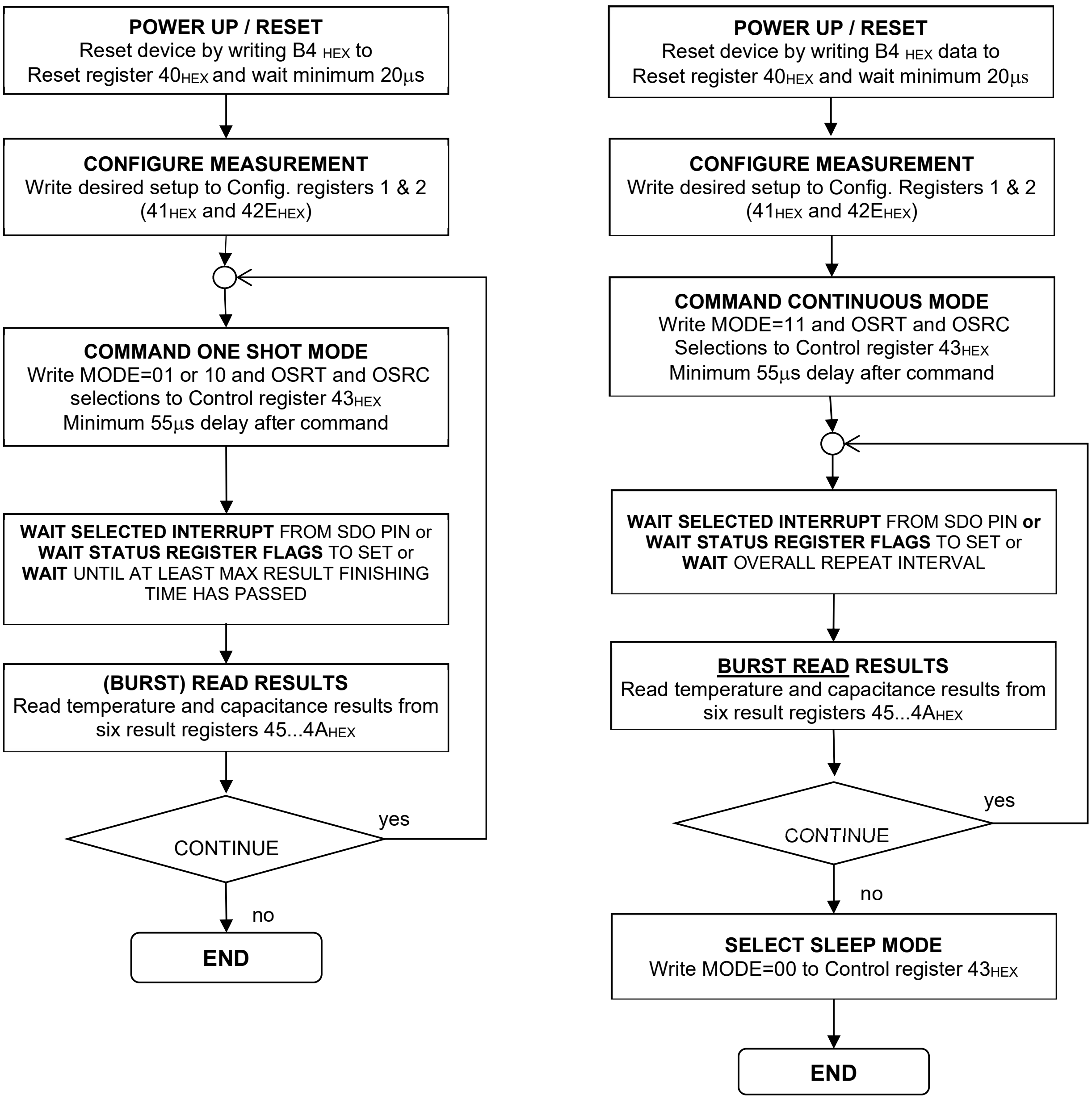


Figure 5. Flow charts for measurement flow of a calibrated MAS6513 sensor system

Figure 5 present flow charts for measurement flow of calibrated MAS6513 sensor system in both one shot mode (single command based measurement) and continuous mode (repeated measurements in a loop). After giving measurement start command there must be minimum 55µs delay before reading from or writing to the MAS6513 since internal data bus is reserved for up to that time after receiving the command.

♦ Alert function

The MAS6513 can be configured to given an alert if any of the selected measurements exceeds programmable alert limits. The alert state is indicated by four MSB bits of the status register which keep track of alert condition occurrence. See also Status register description on page 23.

Additionally, the SDO pin can be configured as an interrupt output for the alert event. The interrupt output can then be used to interrupt microcontroller when measured temperature or capacitance result has exceeded any of the programmable alert limits. This can be a useful feature for example when the MAS6513 is configured to run measurements automatically (continuous measurement mode MODE=11) and if microcontroller attention is required only when an alert is detected.

Important note: The Alert function is accessible only via I2C bus communication since the programmable alert limit registers are located outside address space that is supported by 7-bit register addressing of the SPI bus. See register map table 7 on page 18.

There are 24-bit high and low set limits (HSETx, LSETx) for temperature (x=T) and capacitance (x=C) value. If any measurement result exceeds the set limit the interrupt is set. There are additionally 24-bit high and low clear limits (HCLRx, LCLRx) for temperature (x=T) and capacitance (x=C). If selected measurement results are within clear limits the interrupt is cleared. Separation between set and clear limits defines amount of hysteresis in the alert function. Non-zero hysteresis must be used. Also relative order of alert limits must be as shown in figure 6 i.e. HSETx > HCLRx > LCLRx > LSETx. Note that alert limits are considered as signed integer numbers if calibration calculation is enabled (XCALC=0) but as unsigned numbers if calibration calculation is disabled (XCALC=1). The eight 24-bit programmable alert limits are located in register addresses 80_{HEX}-97_{HEX}. See register map table 7 on page 18.

The alert function is activated by choosing INTSEL=01 or INTSEL=11 in the Configuration register 1 (see table 8 on page 20). To enable interrupt output there is additionally needed to select SDOFS=01. Interrupt output polarity is by default active low (INTLH=0) but it can be also configured to active high (INTLH=1). Note that proper alert limits should be programmed before activating alert function.

When activated the Status register alert bits are set accordingly if any of the selected measurement results exceeds its alert limits. The status register alert bits are cleared only by reading the Status register i.e. measurement results within clear limits do not clear Status register alert bits.

Figure 6 illustrates SDO output operation when interrupt output is enabled (SDOFS=01), active high (INTLH=1) state is selected and alert function is activated by choosing INTSEL=11. The difference between the two alert function options (INTSEL=01 or 11) is how the alert condition is cleared. In both cases the interrupt output is cleared when all selected results are within their clear limits. However, in INTSEL=01 selection the interrupt output can be additionally cleared by reading the Status register. Note that this can lead to oscillation behavior in the interrupt output signal if any measurement result keeps staying outside its set limit and if Status register is read every time the interrupt signal is detected.

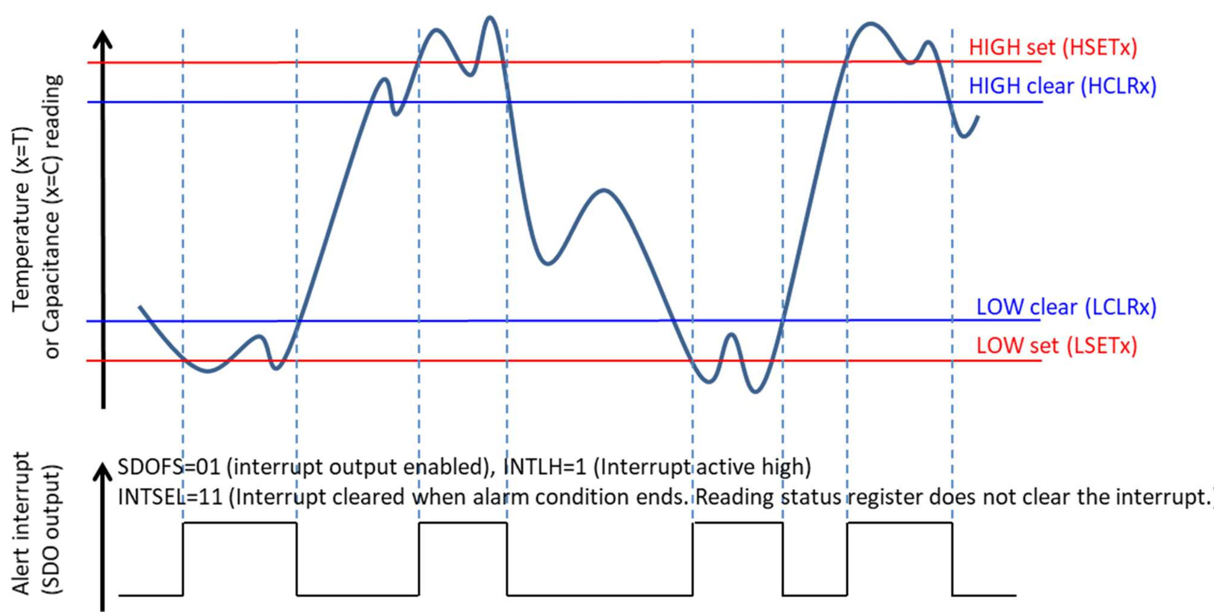


Figure 6. Alert interrupt **output (SDO pin)** operation **at** INTSEL=11**, INTLH=1 selection**

♦ Trimming settings and operating modes

The MAS6513 has four trimming settings. Each setting has storage in both register and EEPROM memory location. The register values determine trimming setting which takes action and the EEPROM serves as non-volatile storage of the trimming values.

Three of the trimming settings are for the capacitive front-end trimming. They comprise of values of two internal offset capacitance matrix values and gain setting. These are used for maximizing measurement resolution by fitting input signal range of MAS6513 with the capacitive sensor's signal range. See tables 19-21 on page 29 for details.

The fourth trimming setting is for internal clock oscillator which should be left untouched since it is factory trimmed. See table 22 on page 30 for details.

MAS6513 has three trimming setting operating modes which are selected by TRIM bits in the Trim and test register (51_{HEX}). See table 14 on page 26. By default, the TRIM=00 which is the normal trimming operating mode in which all the trimming settings and calibration coefficients (if XCALC=0 is additionally selected) will be automatically read from EEPROM memory to registers after each oneshot or continuous measurement command. This guarantees that the internal clock oscillator, capacitive front-end and calibration calculation engine have always proper trimming and calibration coefficient values when the measurements are run. Thus, the end user of a trimmed sensor system only needs to start measurement(s) at the selected configuration settings and read the result(s) when they are available.

The other two trimming setting operating modes are only for searching of the optimal trimming values. In the TRIM=01 (or 10) setting only internal clock oscillator factory trimming setting is read from the EEPROM after the measurement command but the capacitive front-end trimming settings and calibration coefficients are taken from the registers. This allows fast search of trimming settings via registers since the slower EEPROM write procedure is not necessary until the final trimming and calibration coefficient values are found and after which they can be stored to the EEPROM. The third TRIM=11 trimming setting operating mode should not be used since it is only for factory trimming of the internal clock oscillator.

The Trim and test register (51_{HEX}) contains also test mode (TMS) and input data source (SRC) bit settings. These are mainly for testing purposes and default zero bit values are normally used (TMS=00000, SRC=0).

♦ Internal clock oscillator

MAS6513 has an internal clock oscillator making external clock unnecessary. In the one shot mode it is turned on only during the measurements and turned off when the sleep mode is entered. In the continuous mode the internal clock oscillator is turned on continuously to run selected measurements periodically.

The internal oscillator frequency is factory trimmed to 2 MHz using a 7-bit register. See table 22 on page 30 for Clock oscillator frequency trim register ($7F_{HEX}$). The 2's complement format factory trimming value has been stored into EEPROM address ($3F_{HEX}$). Note: it is recommended to not touch the factory trimming value of the internal clock oscillator. The A/D converter runs from a divided system clock which is 125 kHz for capacitance and 250 kHz for temperature.

♦ EEPROM memory

The 512 bit (64 byte) EEPROM memory is available via I2C/SPI serial bus. It is for storing trim and calibration coefficient data on chip.

32 bits (4 bytes) of the EEPROM are reserved for trimming purposes as follows. Two 8 bit trim values are for internal capacitance offset matrices (CS_INT, CR_INT) and one 8 bit trim value is for the gain (GRDAC). One 8 bit trim value (OSCF) is storing factory trim setting of internal 2MHz clock oscillator.

There are three 24 bit calibration coefficients (T0, T1 and T2) reserved for temperature calibration and Nine 24 bit calibration coefficients (C00, C10, C01, C11, C20, C02, C21, C12 and C30) for capacitive sensor calibration. In addition there are 8 bits (1 byte) reserved for programmable alternative I2C device address.

The remaining 184 bits (23 bytes) are free for other use such as storing sensor ID and EEPROM memory CRC check sum information. See table 6 for EEPROM map and table 7 for register map on page 18.

To read from and write to EEPROM requires that VDD, VDDIO and VPP voltages are applied. However, in read only applications the VPP voltage is not needed and it should be connected to ground (GND). See also chapters EEPROM WRITE PROCEDURE and EEPROM READ ONLY PROCEDURE on pages 30-31.

♦ Calibration

MAS6513 is able to output calibrated temperature and capacitive sensor readings. This is accomplished with a 24-bit DSP unit which includes dedicated calibration calculation engine. It can perform second order polynomial linearization for the PTAT temperature sensor signal. The capacitive sensor signal is linearized using third order polynomial and compensated from up to second order temperature dependencies.

To achieve accurate calibrated temperature and capacitive sensor output readings the sensor and MAS6513 have to go through calibration procedure which consists of series of measurements accomplished in pre-determined temperature and sensed sensor parameter (pressure, humidity etc.) conditions. The calibration procedure results up to twelve 24-bit calibration coefficients (up to three for temperature and up to nine for capacitive sensor reading) which are stored to specific EEPROM memory addresses (18_{HEX} – $3B_{HEX}$) that have been reserved for the calibration coefficients.

In addition to calibration coefficients the EEPROM holds 8-bit trim values for the capacitive front-end ($3C_{HEX}$ – $3E_{HEX}$). See EEPROM map in table 6 on page 18.

See next page for an example of MAS6513 based sensor system calibration flow. See also DAEV6513 evaluation board document and sensor calibration excel calculator showing examples how to calculate the calibration coefficients in the MAS6513 based sensor system.

EXAMPLE OF MAS6513 BASED SENSOR SYSTEM CALIBRATION FLOW

1. Initial setup

- Choose most suitable measurement configuration
  - Configuration register 1:
    - XCALC=1 (disabled to get raw ADC values)
    - SDOFS=00 (by default normal SDO pin operation)
    - INLTH=0, INTSEL=00 (by default interrupts disabled)
    - DIV=00 (by default no division if sensed capacitance is less than max 20pF)
  - Configuration register 2:
    - DELAY=000 (no delay by default, this setup concerns only Continuous mode)
    - FILTER=000 (IIR filter disabled)
    - CMM=00 (capacitance difference mode for changing capacitances ∆C from 2pF up to 20pF)
  - Control register:
    - OSRT=OSRC=101 for example i.e. 16x oversampling for good noise resolution
    - MODE=01 for One shot mode
  - Trim and test register: x
    - TMS=00000, SRC=0 for normal operating mode
    - TRIM=01 to select using register values except using EEPROM factory trim value for internal oscillator
- Default configuration for capacitive front-end based on sensor
  - Capacitor matrix register for CS_INT: OCDACS=0 for single capacitor sensor
  - Capacitor matrix register for CR_INT: OCDACR=93 for example for 8pF sensor
  - Gain register: GRDAC=109 for example for ∆C=4pF sensor
  - See also evaluation kit excel calculator tool for initial front-end setup calculation

2. Front-end trim values

- Trim capacitive front-end offset
  - Adjust OCDACR to get raw ADC reading to expected code range at initial sensor and temperature condition (for example)
  - Alternatively, this step can be done as first step in the first calibration condition point

3. Calibration measurements

- Choose calibration points which comprise of combinations of different sensor (humidity, pressure etc.) and temperature conditions
- Number of condition points depends on order of calibration. For example, if second order temperature compensation is needed the calibration points must include minimum three different temperature condition points i.e. one condition point more than order of the calibration.
- Measure raw 24-bit capacitance and temperature readings using MAS6513 in each calibration condition point
- Measure and store sensor condition chamber readings (e.g. humidity or pressure and temperature)
- Averaging of above measurements can be additionally used to improve precision

4. Calculate calibration coefficients

  - Choose integer number output unit values according to desired output resolution (for example target 250 value, if temperature in decimal is 25.0°C but 0.1°C resolution is desired etc.)
- Calculate floating point calibration coefficient values using least squares matrix equation
- Calculate calibration coefficients for temperature and capacitance separately
- Scale floating point numbers into signed 24-bit integers. See chapter "CALIBRATION CALCULATION ENGINE FORMULAS" equations 10a-10l on page 31.
- See also evaluation board excel calculator tool showing examples of calibration coefficient calculations in various order calibration cases

5. Program front-end trim and calibration coefficient values to EEPROM

- Write capacitive front-end (OCDACS, OCDACR, GRDAC) and calibration coefficient (T0-T2, C00-C30) values to EEPROM. See EEPROM write procedure in figure 7 on page 32.

6. Verify sensor accuracy after calibration

- Measure calibrated output readings (XCALC=0, TRIM=00 to enable calculation engine and to use values from EEPROM) by going through sensor (humidity, pressure etc.) and temperature conditions.

EEPROM AND REGISTER MAP

Table 6. EEPROM map (non-volatile memory)

Address [hex]	Name [-]	Access [R/W]	Factory value [hex]	Type [-]	Description [-]
00-16	-	R/W	00	EEPROM	Free EEPROM memory space (23 bytes)
17	ADDR	R/W	factory value EA (75_{HEX} I2C address)	EEPROM	Programmable alternative I2C device address
18-1A	T0	R/W	00	EEPROM	MSB, LSB and XLSB of T0 coefficient
1B-1D	T1	R/W	00	EEPROM	MSB, LSB and XLSB of T1 coefficient
1E-20	T2	R/W	00	EEPROM	MSB, LSB and XLSB of T2 coefficient
21-23	C00	R/W	00	EEPROM	MSB, LSB and XLSB of C00 coefficient
24-26	C10	R/W	00	EEPROM	MSB, LSB and XLSB of C10 coefficient
27-29	C01	R/W	00	EEPROM	MSB, LSB and XLSB of C01 coefficient
2A-2C	C11	R/W	00	EEPROM	MSB, LSB and XLSB of C11 coefficient
2D-2F	C20	R/W	00	EEPROM	MSB, LSB and XLSB of C20 coefficient
30-32	C02	R/W	00	EEPROM	MSB, LSB and XLSB of C02 coefficient
33-35	C21	R/W	00	EEPROM	MSB, LSB and XLSB of C21 coefficient
36-38	C12	R/W	00	EEPROM	MSB, LSB and XLSB of C12 coefficient
39-3B	C30	R/W	00	EEPROM	MSB, LSB and XLSB of C30 coefficient
3C	OCDACS	R/W	00	EEPROM	CS_INT offset capacitor trim data
3D	OCDACR	R/W	00	EEPROM	CR_INT offset capacitor trim data
3E	GRDAC	R/W	00	EEPROM	GAIN trim data
3F	OSCF	R/W	factory trim value	EEPROM	Clock oscillator frequency trim data

Table 7. Register map (volatile memory)

Address [hex]	Name [-]	Access [R/W]	Reset value [hex]	Type [-]	Description [-]
40	RST	W	00	Register	Reset register
41	CFG1	R/W	00	Register	Configuration register 1
42	CFG2	R/W	00	Register	Configuration register 2
43	CTRL	R/W	00	Register	Control register
44	STS	R	00	Register	Status register
45-47	TEMP	R	800000	Register	MSB, LSB and XLSB of temperature result
48-4A	CAP	R	800000	Register	MSB, LSB and XLSB of capacitance result
4B-4D	TSTT	R/W	000000	Register	MSB, LSB and XLSB of temperature test input data
4E-50	TSTC	R/W	000000	Register	MSB, LSB and XLSB of capacitance test input data
51	TSTREG	R/W	00	Register	Trim and test register
57	ADDR	R/W	EC (1)	Register	Programmable alternative I2C device address
58-5A	T0	R/W	000000	Register	MSB, LSB and XLSB of T0 coefficient
5B-5D	T1	R/W	000000	Register	MSB, LSB and XLSB of T1 coefficient
5E-60	T2	R/W	000000	Register	MSB, LSB and XLSB of T2 coefficient
61-63	C00	R/W	000000	Register	MSB, LSB and XLSB of C00 coefficient
64-66	C10	R/W	000000	Register	MSB, LSB and XLSB of C10 coefficient
67-69	C01	R/W	000000	Register	MSB, LSB and XLSB of C01 coefficient
6A-6C	C11	R/W	000000	Register	MSB, LSB and XLSB of C11 coefficient
6D-6F	C20	R/W	000000	Register	MSB, LSB and XLSB of C20 coefficient
70-72	C02	R/W	000000	Register	MSB, LSB and XLSB of C02 coefficient
73-75	C21	R/W	000000	Register	MSB, LSB and XLSB of C21 coefficient
76-78	C12	R/W	000000	Register	MSB, LSB and XLSB of C12 coefficient
79-7B	C30	R/W	000000	Register	MSB, LSB and XLSB of C30 coefficient
7C	OCDACS	R/W	00	Register	CS_INT offset capacitor trim data
7D	OCDACR	R/W	00	Register	CR_INT offset capacitor trim data
7E	GRDAC	R/W	00	Register	GAIN trim data
7F	OSCF	R/W	00	Register	Clock oscillator frequency trim data
80-82	HSETT	R/W	000000	Register	MSB, LSB and XLSB of high set alert limit for temperature result
83-85	HCLRT	R/W	000000	Register	MSB, LSB and XLSB of high clear alert limit for temperature result
86-88	LCLRT	R/W	000000	Register	MSB, LSB and XLSB of low clear alert limit for temperature result
89-8B	LSETT	R/W	000000	Register	MSB, LSB and XLSB of low set alert limit for temperature result
8C-8E	HSETC	R/W	000000	Register	MSB, LSB and XLSB of high set alert limit for capacitance result
8F-91	HCLRC	R/W	000000	Register	MSB, LSB and XLSB of high clear alert limit for capacitance result
92-94	LCLRC	R/W	000000	Register	MSB, LSB and XLSB of low clear alert limit for capacitance result
95-97	LSETC	R/W	000000	Register	MSB, LSB and XLSB of low set alert limit for capacitance result

Note: When using the SPI serial interface the MSB bit of EEPROM or register address is also used for selecting write (0) or read (1) operation. Thus, in SPI read the MSB address bit need to be set 1 in the addresses presented in the tables 6 and 7. For example the CS_INT offset capacitor trim data EEPROM write address is %00111100 = 3C $_{HEX}$ but the EEPROM read address is %10111100 = BC $_{HEX}$ if MSB bit is included to the address value.

Note 1: In power-on-reset (POR) the programmable alternative I2C device address register is set to EC_{HEX} (%1110 1100) value which corresponds to 76_{HEX} (%111 0110) I2C device address in 7-bit notation. However, by giving a software reset (writing $B4_{HEX}$ to Reset register) initiates EEPROM read sequence which sets register value to that of EEPROM address 17_{HEX} value. See Reset register on the next page.

RESET REGISTER (40_{HEX})

The Reset register is for resetting the device via serial bus i.e. giving a software reset. The reset will take place immediately after B4 $_{HEX}$ (1011 0100 $_{BIN}$) is written to the Reset register address 40_{HEX} via the I2C or SPI serial bus interface. Reset initializes internal counters, serial communication bus and all registers from 40_{HEX} to 97_{HEX} to default values. See table 7 for MAS6513 register map and reset values. Additionally, software reset initiates EEPROM read sequence which transfers programmable alternative I2C device address from EEPROM address 17_{HEX} to corresponding register address 57_{HEX}. Thus, to take programmable alternative I2C device address into use there must be given additionally a software reset after every power-up (supply voltage rise) of the device. Note that after software reset there should be minimum 20µs delay before reading from or writing to the MAS6513 to make sure the EEPROM read sequence has been completed.

The programmable alternative I2C device address in the EEPROM has factory set value EA_{HEX} which corresponds to 75_{HEX} I2C address in 7-bit address notation. Thus, after a software reset the MAS6513 will respond to both hardwired I2C address 76_{HEX} and the factory programmed I2C address 75_{HEX}.

CONFIGURATION REGISTER 1 (41_{HEX})

Configuration register 1 (41_{HEX}) contains bits for configuring built-in calibration calculation, SDO pin function, interrupts and capacitance measurement clock division.

The XCALC bit is for enabling built-in calibration calculation. By default, it is enabled (XCALC=0) and calibrated temperature is calculated after every temperature measurement. Similarly calibrated temperature compensated capacitance reading is calculated after every capacitance measurement. Calibrated 24-bit temperature reading is stored to Temperature result registers ($45…47_{HEX}$) and calibrated 24-bit capacitance reading to Capacitance result registers ($48…4A_{HEX}$).

Calibrated readings are calculated using latest ADC results of temperature and capacitance and twelve calibration coefficients (T0-T2, C00-C30) in registers ($58…7B_{HEX}$). By default, the calibration coefficients, capacitive front-end trim settings (OCDACS, OCDACR and GRDAC) and Internal clock oscillator trim setting (OSCF) are transferred from EEPROM address ($18…3F_{HEX}$) and to corresponding registers ($58…7F_{HEX}$) in the end of One shot or Continuous mode start command. This is the default operating mode selected by TRIM=00 setting in the Trim and test register (51_{HEX}). See table 14 on page 26 for other TRIM bit options.

When disabled (XCALC=1) there are no calculations performed and either raw ADC results or filtered raw results (FILTER<>000) are stored to the temperature and capacitance result registers.

The SDOFS bits configure SDO pin function. By default (SDOFS=00) setting the SDO pin has no function in I2C bus communication but in SPI bus communication it operates as serial data output of 4-wire SPI bus. Any other setting (SDOFS<>00) configures SDO pin to other function and in case of SPI bus communication only 3-wire protocol is supported.

By SDOFS=01 selection the SDO pin is configured as interrupt output. Interrupt enable and type of interrupt is selected by INTSEL bits. Interrupt output polarity is selected by INTLH bit. INTSEL=01 or 11 selects interrupt from Alert function and INTSEL=10 interrupt from selected measurements becoming ready for reading.

Selecting SDOFS=10 allows MAS6513 to be operated using external 2MHz clock which is applied to the SDO pin. External clock option can be used for example if A/D conversions need to be synchronized to external clock.

MAS6513 supports two hardware configurable I2C device addresses. By default, the 7-bit I2C device address is 76 $_{HEX}$ (%1110 110). By setting SDOFS=11 the logic state of the SDO pin determines the LSB bit of the I2C device address. This enables using two MAS6513 devices on the same I2C bus when having pull down resistor from SDO to GND in one of the devices with I2C device address 76 $_{HEX}$ (%1110 110) and pull up resistor from SDO to VDDIO in the other device with I2C device address 77 $_{HEX}$ (%1110 111). See figure 11 on page 37. In addition to the hardware configurable I2C device addresses the MAS6513 supports also EEPROM programmable I2C address.

INTSEL bits are for enabling interrupts. By default, the interrupts are disabled (INTSEL=00). When enabled (INTSEL<>0) the SDO pin can be chosen to give an interrupt signal either when selected measurements and calculations are finished or an alert condition has occurred. See table 8 and note 4 on the next page for further details. Interrupt signal polarity is selected by INTLH bit.

The DIV bits define four division options for the capacitance conversion clock frequency; no division or division by 2, 4 or 8. These corresponds to capacitance conversion clock frequencies f_{CLK_CAP} = 125kHz, 62.5kHz, 31.25kHz and 15.625kHz respectively. By default (DIV=00) the capacitance conversion is run at full 125kHz clock frequency. However, if sensor capacitance is larger than 20pF it is necessary to lower clock frequency using the division options. Maximum allowed sensor capacitance is calculated from equation; C_{S_MAX} = 20pF*125kHz / f_{CLK_CAP}. Thus, division by 2 (DIV=01) enables measuring sensor capacitances up to 40pF and maximum division of 8 (DIV=11) enables sensor capacitances up to 160pF. However, note that only sensor base capacitance scales up this much by lower clock frequency but the maximum changing input capacitance range is smaller (see ELECTRICAL CHARACTERISTICS tables).

Table 8. Configuration register 1 (41_{HEX}) description

Bit Number	Bit Name	Description	Value	Function
7	XCALC [(1)]	Enable for calibrated output calculation	0 1	Enabled (default) Disabled
6-5	SDOFS [(2)]	SDO pin function selection	00 01 10 11	SDO output in 4-wire SPI / No function in I2C (default) Interrupt output in I2C/3-wire SPI Input for external 2MHz clock in I2C/3-wire SPI Input for LSB bit of I2C device address in I2C
4	INTLH [(3)]	Interrupt or alert active level selection	0 1	Active low (default) Active high
3-2	INTSEL [(4)]	Interrupt selection	00 01 10 11	Interrupts disabled (default) Interrupt from any selected result exceeding alert limits Alert interrupt is cleared when the alert condition ends or the status register is read Interrupt from selected measurement results ready Interrupt from any selected result exceeding alert limits Alert interrupt is cleared only when the alert condition ends
1-0	DIV [(5)]	Clock division for capacitance conversions	00 01 10 11	No clock division: f_{CLK_CAP} = 125 kHz (default) Clock division by 2: f_{CLK_CAP} = 62.5 kHz Clock division by 4: f_{CLK_CAP} = 31.25 kHz Clock division by 8: f_{CLK_CAP} = 15.625 kHz

Note 1: When enabled (XCALC=0) the calibrated temperature and capacitance calculations are performed after finishing selected A/D conversions. See figures 3-4 on pages 9-10. The calculated output results are signed 24-bit integer numbers. For proper calibrated temperature and capacitance readings there is needed at least one temperature and one capacitance conversion result and proper calibration coefficients stored in the EEPROM memory. When disabled (XCALC=1) the output results are unsigned 24-bit integer numbers.
Note 2: By default (SDOFS=00) the SDO pin is configured as output of 4-wire SPI bus. In this configuration the SDO pin has no function when using I2C bus communication and the SDO pin is at high impedance state. Using any other setting (SDOFS<>00) configures the SDO pin to have other functions as follows. The SDOFS=01 or 10 settings enable 3-wire SPI bus operation by configurig SDI pin communication to be bidirectional. The SDOFS=01 configures SDO as an output for interrupts which are enabled and selected by the INTSEL bits. The SDOFS=10 selects using external clock instead of internal clock oscillator. In this selection an external 2MHz clock signal should be applied to the SDO pin. The SDOFS=11 configures SDO pin as input for determining LSB bit of the I2C bus device address. In this selection external pull up resistor from SDO to VDDIO sets device address to 77 $_{HEX}$ (%1110 111) and external pull-down resistor from SDO to GND sets device address to normal 76 $_{HEX}$ (%1110 110). This configuration allows using two MAS6513 devices on the same I2C bus just by adding necessary pull-up and down resistors. See figure 11 on page 37.
Note 3: By default the interrupt is active low (INTLH=0) i.e. output signal is normally high until in interrupt it goes low. Configuring INTLH=1 selects interrupt active high.
Note 4: By default the interrupts are disabled (INTSEL=00). When enabled (INTSEL<>0) the interrupt can be selected either from alert condition (INTSEL=01 or 11 which also activate alert function) or from selected measurement results becoming ready (INTSEL=10). To get interrupt signal out from SDO pin there needs to be additionally selected SDOFS=01. The INTSEL=01 and INTSEL=11 selections both give interrupt when capacitance or temperature result has exceeded alert limit. The difference between the two alert function options (INTSEL=01 or 11) is how the alert condition is cleared. In both cases the interrupt output is cleared when all selected results are within their clear limits. However, in INTSEL=01 selection the interrupt can be additionally cleared by reading status register. Note that this can lead to oscillation behavior in the interrupt output signal if any new measurement result keeps staying outside its set limit and if status register is read every time the interrupt signal is detected. The INTSEL=10 selection gives interrupt when selected measurements and calculations are finished and results are ready for reading. For example, if INTSEL=10, both temperature and capacitance measurements are selected (OSRT, OSRC<>000) and calculation is enabled (XCALC=0) the interrupt signal will be given only after all measurements and calculations have been finished. Note that reading the selected measurement results makes the interrupt output (SDO pin) to return to inactive state and the interrupt becomes active again when new unread results are available.
Note 5: There are four clock division options (DIV) available for capacitance conversions; Non-divided, division by 2, 4 or 8. Clock division options affect only capacitance conversions and when using either internal (SDOFS<>10) or external clock (SDOFS=10). Non-divided (DIV=00, default) clock frequency for capacitance conversion is f_{CLK_CAP} = 125kHz. Temperature conversions are always run using f_{CLK_TEMP} = 250kHz clock independent of DIV setting. When using clock division it is possible to extend maximum allowed sensor and reference capacitance values by the division factor; C_{S_MAX} = 20pF*125kHz / f_{CLK_CAP}. However, note that maximum changing sensor capacitance does not increased by this factor. Also note that clock division will increase capacitance conversion time according to selected division factor.

CONFIGURATION REGISTER 2 (42_{HEX})

Configuration register 2 (42_{HEX}) contains standby mode delay, digital infinite impulse response (IIR) low pass filter coefficient and capacitance measurement mode configurations. See table 9.

In continuous mode the selected measurements are repeated in a loop. Between measurements there is a delay during which the device enters standby mode. The delay has eight options selectable from 0ms (no delay) up to 2048ms. See delay time (t_{DELAY}) illustration in figure 4 on page 12.

By FILTER setting it is possible to select optional low pass filtering for the temperature and capacitance conversion results. There are eight filter options available from no filtering (default) up to filter coefficient COEFF=128. The low pass filtering can be used to damp sudden variations in the sensor signal and to further improve noise resolution by an additional filtering of the noise. The IIR filter is initialized every time the FILTER value is changed. Writing the same FILTER value to the Configuration register 2 which it already contains does not initialize the filter. The filter does not affect output data rate but it narrows signal bandwidth and increases step response delay. See also APPLICATION INFORMATION on page 48 regarding IIR filter noise resolution improvement and step response characteristics. When selected (FILTER<>000) both temperature and capacitance conversion results are filtered according to equation 1 below. If calibration calculation is disabled (XCALC=1) the filtered 24-bit results are stored to the Temperature result registers ($45\ldots47_{HEX}$) and Capacitance result registers ($48\ldots4A_{HEX}$). If calibration calculation is enabled (XCALC=0) the stored results are calibrated readings which are based on filtered conversion results.

The MAS6513 support three difference capacitance measurement modes; capacitance difference, capacitance ratio and sum of capacitance. Measurement mode is selected by CMM bits. In difference modes (CMM=00 or 01) the output is proportional to capacitance difference (C_S-C_R). In capacitance ratio mode the output is proportional to capacitance ratio (C_S-C_R)/C_S and in sum of capacitance the output is proportional to sum of external sensor capacitances C_{S_EXT}+C_{R_EXT}. The capacitance difference mode has two input capacitance range options. The CMM=00 selects internal reference capacitance CREF=6pF by which changing input capacitance (ΔC) ranges can be covered from 2pF up to 20pF by adjusting the GAIN register GRDAC value (see table 21). The CMM=01 selects internal reference capacitance CREF=3pF by which changing input capacitance ranges from 1pF up to 10pF can be covered. This setting is mainly targeted for narrow 1pF…2pF changing input capacitance ranges.

$$\mathbf{CODE_{NEW}} = \frac{\mathbf{CODE_{OLD}}\cdot(\mathbf{COEFF}-\mathbf{1})+\mathbf{CODE_{ADC}}}{\mathbf{COEFF}}$$

Equation 1

$CODE_{NEW}$ = new filtered output

$CODE_{OLD}$ = previous filtered output

$CODE_{ADC}$ = latest A/D conversion result

COEFF = IIR filter coefficient

Table 9. Configuration register 2 (42_{HEX}) description

Bit Number	Bit Name	Description	Value	Function
7-5	DELAY	Standby mode delay between continuous measurements	000 001 010 011 100 101 110 111	0ms, maximum rate (default) 32 ms 64 ms 128 ms 256 ms 512 ms 1024 ms 2048 ms
4-2	FILTER	IIR filter coefficient	000 001 010 011 100 101 110 111	COEFF=1, no filtering (default) COEFF=2 COEFF=4 COEFF=8 COEFF=16 COEFF=32 COEFF=64 COEFF=128
1-0	CMM	Capacitance measurement mode	00 01 10 11	Capacitance difference converter, CREF=6pF (default) Capacitance difference converter, CREF=3pF Capacitance ratio converter Capacitance sum converter, CREF=6pF

CONTROL REGISTER (43_{HEX})

The Control register (43_{HEX}) is for starting desired measurements and selected resolution.

MODE bits select operation between three different modes. After power on reset the device is in sleep mode (MODE=00) in which it does not perform any function and consumes only very small leakage current. The one shot mode is selected by MODE=01 or 10 setting. In this mode The MAS6513 performs selected measurements only once after which it returns back to sleep mode. The continuous mode is selected by MODE=11. In this mode the selected measurements are cycled in a loop until MODE=00 setting is written to the Control register.

There are eight oversampling ratio (OSR) settings available for both temperature and capacitance measurements. The OSRT is for temperature and OSRC for capacitance measurements. These are for selecting desired measurements and their resolution. Higher OSR setting corresponds to higher resolution but also to higher power consumption and longer conversion time and vice versa. This makes it possible to optimize resolution, power consumption and conversion time in each application. See ELECTRICAL CHARACTERISTICS for further details.

Starting measurements requires setting MODE<>00 and selecting desired measurements by setting OSRT<>000 or/and OSRC<>000.

Table 10. Control register (43_{HEX}) description

Bit Number	Bit Name	Description	Value	Function
7-5	OSRT	Oversampling ratio for temperature measurement	000 001 010 011 100 101 110 111	No temperature measurement (default) OSR=1x Lowest power OSR=2x Very low power OSR=4x Low power OSR=8x Standard resolution OSR=16x High resolution OSR=32x Very high resolution OSR=64x Highest resolution
4-2	OSRC	Oversampling ratio for capacitance measurement	000 001 010 011 100 101 110 111	No capacitance measurement (default) OSR=1x Lowest power OSR=2x Very low power OSR=4x Low power OSR=8x Standard resolution OSR=16x High resolution OSR=32x Very high resolution OSR=64x Highest resolution
1-0	MODE	Operating mode	00 01, 10 11	Sleep mode (default) One shot mode Continuous mode

STATUS REGISTER (44_{HEX})

The Status register (44_{HEX}) contains various status flags. See table 11.

When alert function has been activated (INTSEL=01 or 11) the four MSB bits indicate whether there has occurred an alert due to measurement result exceeding programmable set limits. There are bits for both temperature (ALRTHT, ALRTLT) and capacitance (ALRTHC, ALRTLC) measurement and for high and low limit alert indication. Note that the Status register alert bits are cleared only by reading from the Status register. Thus, the alert bits are not cleared even if measurement results have returned within clear limits. See chapter "Alert function" on page 14 and register map table 7 on page 18 for programmable alert limits in addresses 80_{HEX}-97_{HEX}.

The RDYADC flag indicates whether A/D conversion is not running (0) or when it is busy (1).

The RDYCLC flag indicates whether calibration calculation is not running (0) or when it is busy (1).

The RDYT and RDYC flags indicate when unread temperature and capacitance results are available at the Result registers. Polling status of these two flags can be used to decide when to read out the new results. Reading data from any of the three Temperature result registers ($45…47_{HEX}$) clears the RDYT flag (RDYT=0). Reading data from any of the three Capacitance result registers ($48…4A_{HEX}$) clears the RDYC flag (RDYC=0).

Table 11. Status register (44_{HEX})

Bit Number	Bit Name	Description	Value	Function
7	ALRTHT		0 1	No T high limit alert T high limit alert
6	ALRTLT		0 1	No T low limit alert T low limit alert
5	ALRTHC		0 1	No C high limit alert C high limit alert
4	ALRTLC		0 1	No C low limit alert C low limit alert
3	RDYADC		0 1	A/D conversion ready A/D conversion busy
2	RDYCLC		0 1	Calculation ready Calculation busy
1	RDYT		0 1	No unread T result available Unread T result available
0	RDYC		0 1	No unread C result available Unread C result available

Note: T = temperature, C = capacitance

TEMPERATURE RESULT REGISTERS ($45…47_{HEX}$)

The content of Temperature result registers depends on FILTER and XCALC settings as follows.

Table 12. Temperature result register ($45…47_{HEX}$) content depending on XCALC and FILTER setting

XCALC	FILTER	Description
0	000	Calibrated temperature calculated from raw ADC result of temperature
0	<> 000	Calibrated temperature calculated from filtered ADC result of temperature
1	000	Raw ADC result of temperature
1	<> 000	Filtered ADC result of temperature

The 24-bit temperature result is stored into three 8-bit registers. The MSB (most significant byte) is at 45_{HEX}, LSB (least significant byte) at 46_{HEX} and XLSB (extra least significant byte) at 47_{HEX}.

CAPACITANCE RESULT REGISTERS ($48…4A_{HEX}$)

The content of Capacitance result registers depends on FILTER and XCALC settings as follows.

Table 13. Capacitance result register ($48…4A_{HEX}$) content depending on XCALC and FILTER setting

XCALC	FILTER	Description
0	000	Calibrated capacitance calculated from raw ADC result of capacitance
0	<> 000	Calibrated capacitance calculated from filtered ADC result of capacitance
1	000	Raw ADC result of capacitance
1	<> 000	Filtered ADC result of capacitance

The 24-bit capacitance result is stored into three 8-bit registers. The MSB (most significant byte) is at 48_{HEX}, LSB (least significant byte) at 49_{HEX} and XLSB (extra least significant byte) at $4A_{HEX}$.

TEMPERATURE TEST INPUT DATA REGISTERS ($4B…4D_{HEX}$)

The three bytes of Temperature test input data registers ($4B…4D_{HEX}$) are for testing purpose only. By the Trim and test register (51_{HEX}) setting SRC=1 it is possible to choose taking temperature and capacitance data for the IIR filtering and calibration calculation from the Temperature and Capacitance test input data registers instead of using corresponding A/D conversion results. This test mode allows testing both IIR filter and calibration calculation with any 24-bit input data. In normal operation (SRC=0) the input data for the IIR filters or calibration calculation are the latest temperature and capacitance conversion results.
XCALC and FILTER settings define type of temperature result which is stored to the Temperature result registers ($45…47_{HEX}$). See table 12 above.

CAPACITANCE TEST INPUT DATA REGISTERS ($4E…50_{HEX}$)

The three bytes of Capacitance test input data registers ($C4E…50_{HEX}$) are for testing purpose only. By the Trim and test register (51_{HEX}) setting SRC=1 it is possible to choose taking temperature and capacitance data for the IIR filtering and calibration calculation from the Temperature and Capacitance test input data registers instead of using corresponding A/D conversion results. This test mode allows testing both IIR filter and calibration calculation with any 24-bit input data. In normal operation (SRC=0) the input data for the IIR filters or calibration calculation are the latest temperature and capacitance conversion results.
XCALC and FILTER settings define type of capacitance result which is stored to the Capacitance result registers ($48…4A_{HEX}$). See table 13 above.

TRIM AND TEST REGISTER (51_{HEX})

After power up the Trim and test register (51_{HEX}) is at reset value 00_{HEX} which selects normal device operation (TMS=00000, SRC=0, TRIM=00). See table 14 on the next page. In the normal operating mode the internal clock oscillator is turned on only during measurements and the CSB and SDO pins have normal function (enabled for SPI communication). Also writing byte to EEPROM will perform automatically byte erase prior byte write (Test mode 0: TMS=00000). Note that SDO pin function is configurable via SDOFS bits in the Configuration register 1 (see table 8 on page 20). In this normal operation the IIR filter uses A/D conversion results for the filtering (SRC=0) and all trim data and calibration coefficients are based on values which are stored to the EEPROM (TRIM=00).

The internal clock oscillator can be turned on all the time and outputted from the SDO pin by selecting test mode 12 (TMS=01100). This setting overrides SDO pin configuration by SDOFS bits in the Configuration register 1 except that an external clock selection (SDOFS=10) should not be used if the internal clock oscillator is wanted to be kept turned on. This test mode is for internal clock oscillator trimming purpose only. Normally (Test mode 0: TMS=00000) and when external clock is not selected (SDOFS<>10) the internal clock oscillator is turned on only during the measurements to save power.

The TMS bits are used for selecting different mainly test purpose modes including EEPROM testing and connecting internal signals to the CSB and SDO pins.

The SRC bit selects input data source for the IIR low pass filter (FILTER<>000) and calibration calculation (XCALC=0). By default SRC=0 which selects input data taken from the A/D conversion results. However, SRC=1 selects to take input data from the Temperature ($4B…4D_{HEX}$) and Capacitance input data registers ($4E…50_{HEX}$) instead. This test mode allows testing of the IIR low pass filter with any 24-bit input data.

The TRIM bits select source of the capacitive front-end and internal clock oscillator trim data and calibration coefficient data. In default normal operating mode (TRIM=00) all trim and calibration data is transferred automatically from EEPROM to corresponding registers in the end of each One shot or Continuous mode command. This is proper operating mode of a trimmed and calibrated sensor module.

The TRIM=01 or 10 setting selects mode which is used in the trimming of the capacitive front-end and calibration of the sensor. In this mode only internal factory trimmed clock oscillator trim data (OSCF) is taken from the EEPROM and the capacitive front-end trim data (OCDACS, OCDACR, GRDAC) and calibration coefficient (T0-T2, C00-C30) values are taken from the registers. Trimming using registers can be done much faster than when using EEPROM since register write does not need the minimum 30ms wait after each byte write which EEPROM requires. After finding optimal front-end trim and calibration coefficient values they need to be written to the non-volatile EEPROM memory. See capacitive front-end offset and gain trimming register tables 19-21 on page 29 and calibration coefficient registers and EEPROM tables 17-18 on page 28.

The TRIM=11 setting selects taking all trim data from registers. This is only for internal clock oscillator trimming purpose and not needed since the internal clock oscillator is factory trimmed.

Table 14. MAS6513 Trim and test register (51_{HEX}) description

Bit Number	Bit Name	Description	Value	Function		
7-3	TMS	Test mode selection		**CSB pin**	**SDO pin**	
		Test mode 0	00000	I: CSB	Note 1	Normal operating mode (default) (EEPROM erase+write in write)
		Test mode 1	00001	I: CSB	Note 1	EEPROM write byte w/o erase
		Test mode 2	00010	I: CSB	Note 1	EEPROM erase byte in write
		Test mode 3	00011	I: CSB	Note 1	EEPROM erase all in write
		Test mode 4	00100	I: CSB	Note 1	-
		Test mode 5	00101	I: CSB	Note 1	-10% input signal for ADC
		Test mode 6	00110	I: CSB	Note 1	10% input signal for ADC
		Test mode 7	00111	I: CSB	Note 1	30% input signal for ADC
		Test mode 8	01000	I: CSB	Note 1	50% input signal for ADC (4)
		Test mode 9	01001	I: CSB	Note 1	70% input signal for ADC
		Test mode 10	01010	I: CSB	Note 1	90% input signal for ADC
		Test mode 11	01011	I: CSB	Note 1	110% input signal for ADC
		Test mode 12	01100	I: CSB	O: INT_OSC (2)	Oscillator trim (OSC on always)
		Test mode 13	01101	I: CSB	Note 1	External clock non-divided
		Test mode 14	01110	I: CSB	Note 1	
		Test mode 15	01111	I: CSB	Note 1	
		Test mode 16	10000	O: VBG	Note 1	VBG test
		Test mode 17	10001	O: VREG	Note 1	VREG test
		Test mode 18	10010	O: SDM	Note 1	SDM test
		Test mode 19	10011	O: RDYADC	Note 1	RDYADC test
		Test mode 20	10100	O: RDYCLC	Note 1	RDYCLC test
		Test mode 21	10101	O: VTESTP (4)	O: VTESTN (4)	-10% input signal for ADC
		Test mode 22	10110	O: VTESTP (4)	O: VTESTN (4)	10% input signal for ADC
		Test mode 23	10111	O: VTESTP (4)	O: VTESTN (4)	30% input signal for ADC
		Test mode 24	11000	O: VTESTP (4)	O: VTESTN (3,4)	50% input signal for ADC (4)
		Test mode 25	11001		Note 1	-
		Test mode 26	11010		Note 1	-
		Test mode 27	11011		Note 1	-
		Test mode 28	11100	I: VTESTP (5)	I: VTESTN (5)	External input signal for ADC
		Test mode 29	11101	I: CSB	Note 1	EEPROM write with 10ms pulse
		Test mode 30	11110	I: CSB	Note 1	EEPROM write with 25ms pulse
		Test mode 31	11111	I: CSB	Note 1	EEPROM write with 50ms pulse
2	SRC (6)	Selection for input data source of IIR filter and calibration calculation	0 1	Normal operation (default) Select test data input instead of raw ADC results for IIR/calculation		
1-0	TRIM	Selects source of trim data	00 01, 10 11	All trim and calibration coefficient data from EEPROM (default) Only factory OSC trim data from EEPROM All trim and calibration coefficient data from registers		

Note: In test modes (TMS<>00000) the 250kΩ pull-up resistor between CSB and VDDIO pins is disconnected. The VDDIO should be kept above or minimum the regulator voltage (typ 1.8V) since there is ESD diode from both CSB and SDO pins to VDDIO and in test mode they can output signals up to regulator voltage level.
Note 1: The SDO pin function depends on Configuration register 1 (41_{HEX}) SDOFS bit setting. See table 8 on page 20. However, the SDOFS setting is overridden in test modes 12, 21-24 and 28 in which SDO pin signal is determined by test mode according to table 14. When external 2MHz clock is selected (SDOFS=10) the clock frequency is divided by 16 in capacitance conversion and by 8 temperature conversion except in test mode 13 (TMS=01101) which does not have clock frequency division. This test mode is for fast conversion logic testing.
Note 2: In test mode 12 (TMS=01100) the internal oscillator is turned on all the time. This setting overrides SDOFS bit configuration of the SDO pin except that an external oscillator should not be selected (SDOFS=10) since that would turn off the internal oscillator.
Note 3: 50% input signal is produced by internal short between the inputs of the ADC.
Note 4: VTESTP and VTESTN signal are static voltages produce by internal resistor tree. There is no need to start conversion to output these signals.
Note 5: The differential input signal range (ISR=VTESTP-VTESTN) of ADC is ±720mV at V_{REG}=1.8V.
Note 6: Writing six bytes to the Temperature ($4B…4D_{HEX}$) and Capacitance test input data registers ($4E…50_{HEX}$) triggers selected filtering (FILTER<>000) and calibration calculation (XCALC=0) operations if Test data input operating mode has been selected by SRC=1.

PROGRAMMABLE ALTERNATIVE I2C DEVICE ADDRESS REGISTER (57_{HEX})

The MAS6513 supports programmable alternative I2C device address feature which allows connecting several MAS6513 devices on the same I2C bus. However, this requires having each device pre-programmed to unique alternative I2C device addresses before connecting them on the same bus.

After power-up the MAS6513 answers to its default hard wired address 76_{HEX} (%1110 110). After giving a software reset (see RESET REGISTER on page 19) the MAS6513 answers additionally to device address which is found from the EEPROM address 17_{HEX} which holds value of the programmable alternative I2C device address. This is because the software reset not only reset registers to their default values but it also initiates EEPROM read sequence which transfers programmable alternative I2C address value from EEPROM to the corresponding register address 57_{HEX}. Thus, to take programmable alternative I2C device address feature into use it is necessary to give a software reset after every power-up.

The programmable alternative I2C device address value in EEPROM is factory programmed to EA_{HEX} (%1110 1010) value which corresponds to the default 75_{HEX} (%111 0101) device address in 7-bit notation.

Tables 15 and 16 present contents of Programmable alternative I2C device address in register and EEPROM.

Table 15. Programmable alternative I2C device address register (57_{HEX})

A7	A6	A5	A4	A3	A2	A1	A0	Description
1	1	1	0	1	1	0	0	Power-up value (EC $_{HEX}$ which corresponds to 76_{HEX} in 7-bit notation)
a7	a6	a5	a4	a3	a2	a1	a0	After software reset value from EEPROM address 17_{HEX}

Table 16. Programmable alternative I2C device address in EEPROM (17_{HEX})

A7	A6	A5	A4	A3	A2	A1	A0	Description
1	1	1	0	1	0	1	0	Factory programmed value (EA $_{HEX}$ which corresponds to 75_{HEX} in 7-bit notation)

CALIBRATION COEFFICIENT REGISTERS (58…7B$_{HEX}$)

Table 17. Calibration coefficient registers (58…7B$_{HEX}$)

Coefficient	Bit Number	MSB address	LSB address	XLSB address	Description
T0	23-0	58$_{HEX}$	59$_{HEX}$	5A $_{HEX}$	Temperature offset
T1	23-0	5B$_{HEX}$	5C$_{HEX}$	5D $_{HEX}$	Temperature slope
T2	23-0	5E$_{HEX}$	5F$_{HEX}$	60 $_{HEX}$	Temperature linearization
C00	23-0	61$_{HEX}$	62$_{HEX}$	63$_{HEX}$	Capacitance offset
C10	23-0	64$_{HEX}$	65$_{HEX}$	66$_{HEX}$	Capacitance slope
C01	23-0	67$_{HEX}$	68$_{HEX}$	69$_{HEX}$	Temp dependency of capacitance
C11	23-0	6A$_{HEX}$	6B$_{HEX}$	6C$_{HEX}$	Temp dependency of capacitance slope
C20	23-0	6D$_{HEX}$	6E$_{HEX}$	6F$_{HEX}$	2nd order non-linearity of capacitance
C02	23-0	70$_{HEX}$	71$_{HEX}$	72$_{HEX}$	2nd order temp dependency of capacitance
C21	23-0	73$_{HEX}$	74$_{HEX}$	75$_{HEX}$	Temp dependency of capacitance 2nd order non-linearity
C12	23-0	76$_{HEX}$	77$_{HEX}$	78$_{HEX}$	2nd order temp dependency of cap slope
C30	23-0	79$_{HEX}$	7A$_{HEX}$	7B$_{HEX}$	3rd order non-linearity of capacitance

Each calibration coefficient has non-volatile storage address in the EEPROM memory as presented in table 18. See also EEPROM memory map table 6 on page 18.

All calibration coefficients (and capacitive front-end and internal oscillator trimming values) are automatically transferred from the EEPROM to the corresponding registers right after each One shot (MODE=01 or 10) or Continuous (MODE=11) mode command given using Control register (see table 10 on page 22).

Table 18. Calibration coefficient EEPROM addresses (18…3B$_{HEX}$),

Coefficient	Bit Number	MSB address	LSB address	XLSB address	Description
T0	23-0	18$_{HEX}$	19$_{HEX}$	1A$_{HEX}$	Temperature offset
T1	23-0	1B$_{HEX}$	1C$_{HEX}$	1D$_{HEX}$	Temperature slope
T2	23-0	1E$_{HEX}$	1F$_{HEX}$	20$_{HEX}$	Temperature linearization
C00	23-0	21$_{HEX}$	22$_{HEX}$	23$_{HEX}$	Capacitance offset
C10	23-0	24$_{HEX}$	25$_{HEX}$	26$_{HEX}$	Capacitance slope
C01	23-0	27$_{HEX}$	28$_{HEX}$	29$_{HEX}$	Temp dependency of capacitance
C11	23-0	2A$_{HEX}$	2B$_{HEX}$	2C$_{HEX}$	Temp dependency of capacitance slope
C20	23-0	2D$_{HEX}$	2E$_{HEX}$	2F$_{HEX}$	2nd order non-linearity of capacitance
C02	23-0	30$_{HEX}$	31$_{HEX}$	32$_{HEX}$	2nd order temp dependency of capacitance
C21	23-0	33$_{HEX}$	34$_{HEX}$	35$_{HEX}$	Temp dependency of capacitance 2nd order non-linearity
C12	23-0	36$_{HEX}$	37$_{HEX}$	38$_{HEX}$	2nd order temp dependency of cap slope
C30	23-0	39$_{HEX}$	3A$_{HEX}$	3B$_{HEX}$	3rd order non-linearity of capacitance

INTERNAL CS AND CR CAPACITOR MATRIX REGISTERS (7C$_{HEX}$ AND 7D$_{HEX}$)

There are two internal capacitor matrices C_{S_INT} and C_{R_INT} that add capacitance in parallel to external sensor capacitor (C_{S_EXT}) and external reference capacitor (C_{R_EXT}) respectively. See application figures 15-16 on page 46. These offset capacitances are used to adjust the sensor signal to an optimal CDC input range. Each capacitor matrix has a selectable capacitance from 0pF up to 22pF in typical 86.3fF steps. The three sigma process variation of the capacitor matrix capacitance is ±15%.

The C_{S_INT} capacitor matrix is controlled by 8-bit register (7C$_{HEX}$) value OCDACS. See table 19. It has a corresponding EEPROM address (3C$_{HEX}$) as non-volatile storage of the trim value. The C_{R_INT} capacitor matrix is controlled by 8-bit register (7E$_{HEX}$) value OCDACR. See table 20. It has also corresponding EEPROM address (3D$_{HEX}$) as non-volatile storage of the trim value. The internal C_{S_INT} and C_{R_INT} capacitor matrix capacitance values depend on OCDACS and OCDACR register values according to equations 2-3.

After finding suitable C_{S_INT} and C_{R_INT} capacitor matrix register values the trim values can be stored in the corresponding non-volatile EEPROM addresses.

In normal operating mode (TRIM=00) these trim values are automatically read from the EEPROM and written to the corresponding registers in the end of each One shot or Continuous mode command. See also Trim and test register (51$_{HEX}$) table 14 on page 26 for other trim value operating modes.

$$C_{S\_INT} = 22\,pF \cdot \frac{OCDACS}{255}$$ **Equation 2.**

$$C_{R\_INT} = 22\,pF \cdot \frac{OCDACR}{255}$$ **Equation 3.**

Table 19. C_{S_INT} internal capacitor matrix register (7C$_{HEX}$), EEPROM address (3C$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACS	CDAC control bits	00$_{HEX}$…FF$_{HEX}$	C_{S_INT} offset trimming

Table 20. C_{R_INT} internal capacitor matrix register (7D$_{HEX}$), EEPROM address (3D$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACR	CDAC control bits	00$_{HEX}$…FF$_{HEX}$	C_{R_INT} offset trimming

GAIN REGISTER (7E$_{HEX}$)

The 8-bit gain register value (GRDAC) adjusts excitation signal level for the capacitive sensor. See table 21. Larger register value corresponds to smaller changing input capacitance range and vice versa. The gain register together with the C_{S_INT} and the C_{R_INT} capacitor matrix trim parameters define input capacitance range of measurement. In ideal case the sensor signal is fit perfectly within the linear input capacitance range of the CDC. Such trimming maximizes resolution and dynamic range of the measurement.

The gain register (7E$_{HEX}$) has a corresponding EEPROM address (3E$_{HEX}$) as non-volatile storage of the trim value. After finding a suitable gain register value it can be stored in the non-volatile EEPROM memory. In normal operating mode (TRIM=00) the gain trim value is read automatically from the EEPROM in the end of each One shot or Continuous mode command.

Table 21. Gain register (7E$_{HEX}$), EEPROM address (3E$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-0	GRDAC	RDAC control bits	00$_{HEX}$…FF$_{HEX}$	Gain adjustment by sensor excitation signal level control

CLOCK OSCILLATOR FREQUENCY TRIM REGISTER ($7F_{HEX}$)

Note that the internal clock oscillator frequency has been factory trimmed and the trim value has been stored in the EEPROM ($3F_{HEX}$). It is recommended not to change the factory programmed value!

The clock oscillator frequency trim register ($7F_{HEX}$) is for trimming the internal clock oscillator to 2MHz frequency. To force the internal clock oscillator continuously on and output it from the SDO pin it is necessary to select test mode 12 (TMS=01100) in the Trim and test register (table 14 on page 26). This test mode overrides the SDO pin configuration of the SDOFS bits in the Configuration register 1 (table 8 on page 20).

Oscillator is trimmed using seven trim bits which adjust oscillator period in 6.2 ns steps. Oscillator trim value uses 2's complement format. See table 22. Clock oscillator period decreases when the trim value increases. Typically, a register value of 00_{HEX} corresponds to the nominal 2MHz clock oscillator frequency. After finding a suitable trim value it can be stored to the EEPROM ($3F_{HEX}$).

Table 22. Clock oscillator frequency trim register ($7F_{HEX}$), EEPROM address ($3F_{HEX}$)

Bit Number	Bit Name	Description	Value (bin)	Value (2's complement)	Value (hex)	Value (dec)	Function
7							
6-0	OSCF	Clock oscillator frequency control	0111111 0111110 ……. 0000001 0000000 1111111 1111110 ……. 1000001 1000000	63 62 … 1 0 -1 -2 … -63 -64	3F 3E … 1 0 7F 7E … 41 40	63 62 … 1 0 127 126 … 65 64	Max frequency … … … 2 MHz … … … … Min frequency

Note: Select Test mode 12 (TMS=01100) in the Trim and test register to output 2MHz clock from SDO pin

CALIBRATION CALCULATION ENGINE FORMULAS

When enabled (XCALC=0) calibration calculation engine performs calculations of calibrated temperature and capacitance readings by using A/D conversion results of both temperature and capacitance and twelve calibration coefficients. Since all calculations are based on signed 24-bit integer numbers using 2's complement number representation the calculation engine converts the raw unsigned 24-bit A/D results (ADCraw, ADTraw) to signed numbers (ADC, ADT) by subtraction of value 2^{23} prior actual calibration calculations. See equations 4-5.

$ADT=ADTraw-2^{23}$ **Equation 4.**

$ADC=ADCraw-2^{23}$ **Equation 5.**

The signed integer calibration coefficients are denoted below with upper-case letters (T0, T1, T2, C00, C01, C10, C11, C02, C20, C12, C21, C30). The corresponding floating-point calibration coefficients are denoted with lower-case letters (t0, t1, t2, c00, c01, c10, c11, c02, c20, c12, c21, c30).

MAS6513 does calibrated temperature (T_{CAL}) and capacitance (C_{CAL}) reading calculations based on following two formulas 6-7. After every multiplication there is done division by 2^{24} to keep the numbers within range of 24-bit numbers.

Temperature sensor calibration supports up to 2nd order linearization. See equation 6.

$T_{CAL}=T0+T1*ADT/2^{24}+T2*ADT^2/2^{48}$ **Equation 6.**

Capacitance value calibration supports up to 3rd order linearization and up to 2nd order temperature compensation. See equation 7.

$C_{CAL}=C00+C01*ADT/2^{24}+C10*ADC/2^{24}+C11*ADC*ADT/2^{48}+C02*ADT^2/2^{48}+$ **Equation 7.**
$+C20*ADC^2/2^{48}+C12*ADC*ADT^2/2^{72}+C21*ADC^2*ADT/2^{72}+C30*ADC^3/2^{72}$

Corresponding floating-point calibration coefficient (t0, t1, t2, c00, c01, c10, c11, c02, c20, c12) based equations are as follows.

$T_{CAL}=t0+t1*ADT+t2*ADT^2$ **Equation 8.**

$C_{CAL}=c00+c01*ADT+c10*ADC+c11*ADC*ADT+c02*ADT^2+$ **Equation 9.**
$+c20*ADC^2+c12*ADC*ADT^2+c21*ADC^2*ADT+c30*ADC^3$

The relation between integer (Ax, Cxy) and floating-point (ax, cxy) calibration coefficients is as follows.

$T0=t0$ **Equation 10a.**
$T1=t1*2^{24}$ **Equation 10b.**
$T2=t2*2^{48}$ **Equation 10c.**
$C00=c00$ **Equation 10d.**
$C01=c01*2^{24}$ **Equation 10e.**
$C10=c10*2^{24}$ **Equation 10f.**
$C11=c11*2^{48}$ **Equation 10g.**
$C02=c02*2^{48}$ **Equation 10h.**
$C20=c20*2^{48}$ **Equation 10i.**
$C12=c12*2^{72}$ **Equation 10j.**
$C21=c21*2^{72}$ **Equation 10k.**
$C30=c30*2^{72}$ **Equation 10l.**

EEPROM WRITE PROCEDURE

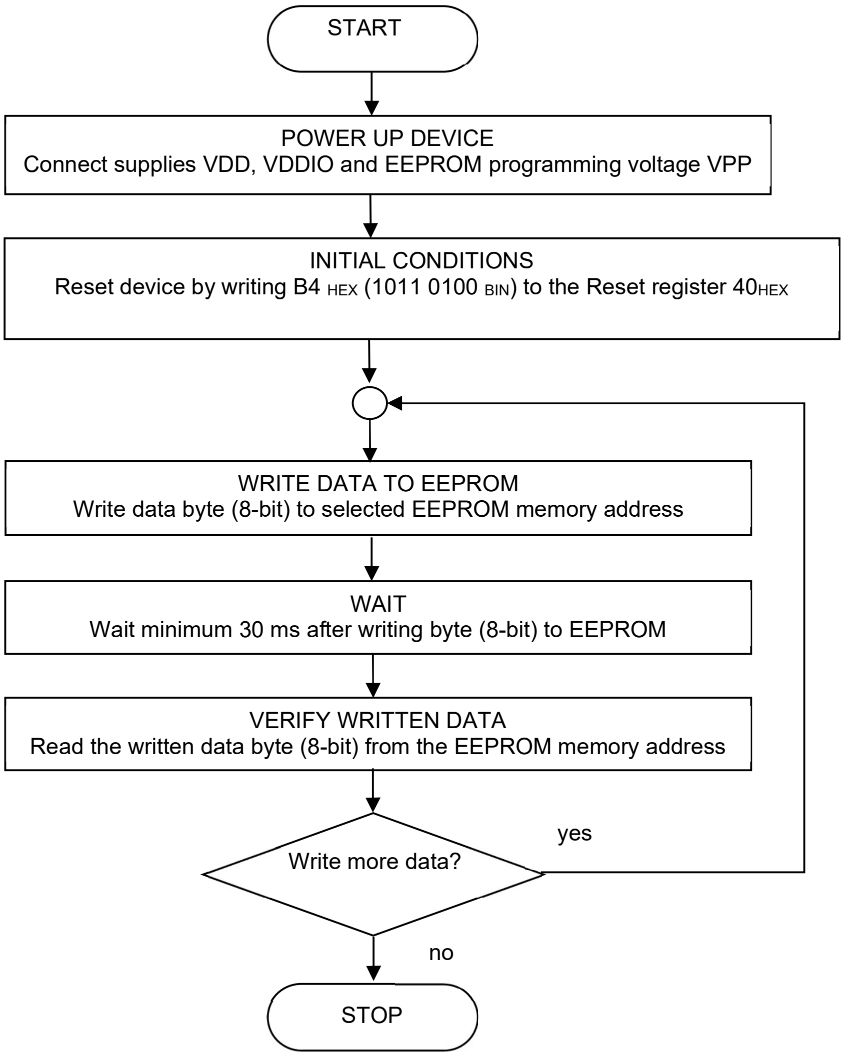


Figure 7. Flow chart for MAS6513 EEPROM write procedure

The MAS6513 has a 512 bit (64 byte) EEPROM memory. 328 bits (41 bytes) are reserved for trimming, calibration coefficient and programmable alternative I2C device address data. The remaining 184 bits (23 bytes) are free for other use such as storing device ID and EEPROM memory CRC check sum information.

Writing to EEPROM memory requires only that proper supply voltages VDD and VDDIO and EEPROM programming voltage VPP are applied. Connecting VDD and VDDIO triggers power-on-reset (POR) but to make sure the device is reset an additional reset can be given by writing $B4_{HEX}$ ($1011\ 0100_{BIN}$) to the Reset register (40_{HEX}). Device reset guarantees that TMS=00000 is selected in the Trim and test register (51_{HEX}) and which selects normal EEPROM write operation to be used in the EEPROM write.

Next the desired data can be written to the EEPROM memory one byte (8-bit) at a time. It is necessary to have a wait of minimum 30 ms after programming each byte (8-bit). The success of each write can be verified by reading back the data (8-bit) and comparing it to the original byte (8-bit). See figure 7 showing the EEPROM write procedure.

Connecting programming voltage VPP to ground (GND) protects the EEPROM from write and erasing. Thus, in read only applications the VPP pin should be always connected to ground (GND).

See also table 6 on page 18 presenting the MAS6513 EEPROM map.

EEPROM READ ONLY PROCEDURE

Reading from EEPROM requires only that proper supply voltages VDD and VDDIO are applied. The EEPROM programming voltage VPP is not necessary and in read only applications it should be connected to ground (GND). That protects the EEPROM memory from write or erasing.

Connecting VDD and VDDIO triggers power-on-reset (POR) but to make sure the device is reset an additional reset can be given by writing B4 $_{HEX}$ (1011 0100 $_{BIN}$) to the Reset register 40_{HEX}.

Next the desired data can be read from the EEPROM memory. In read there is no need for extra wait between reads of each byte like in write. It is also possible to read all EEPROM content in a single read sequence or a “burst” just by continuing the read sequence since after each read byte the read address is incremented automatically to point to the next address. See figure 8 showing the EEPROM read only procedure.

See also table 6 on page 18 presenting the MAS6513 EEPROM map.

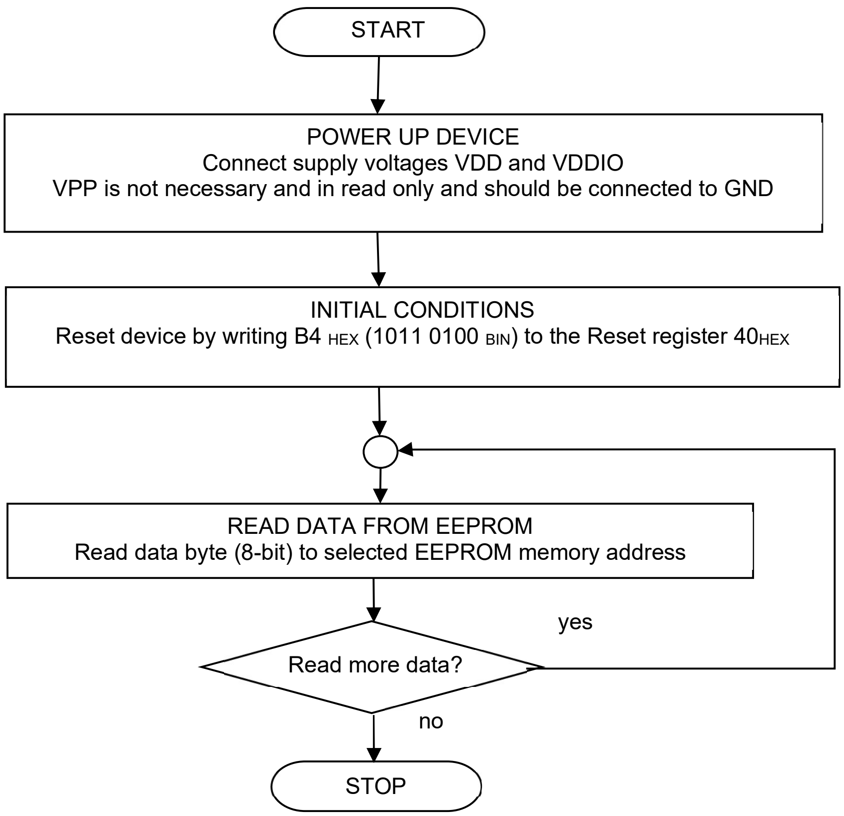


Figure 8. Flow chart for MAS6513 EEPROM read only procedure

SERIAL DATA INTERFACE CONTROL

Serial Interface

The MAS6513 is operated either via 2-wire serial I2C bus or via 3-/4-wire serial SPI bus. Serial bus is for writing configuration data to sensor interface IC and reading out measurement results when they are available. The serial interface is used also for storing capacitive front-end trimming and calibration coefficient data to the non-volatile EEPROM memory.

The 2-wire serial I2C bus type interface comprises of serial clock input (SCK) and bi-directional serial data (SDI) input/output.

Note: The 2-wire I2C bus of MAS6513 supports only basic I2C bus communication protocol but not for example 10-bit addressing and clock stretching features of the I2C bus specification.

The alternative 4-wire serial SPI bus type interface comprises of serial clock input (SCK), serial data input (SDI), serial data output (SDO) and chip select input (CSB). The SPI bus can be configured also to 3-wire SPI bus operation in which the SDI line functions as bidirectional data line.

After power-up (rise of supplies) the MAS6513 is ready to operate via I2C bus 4-wire serial bus protocol. Writing to device using 3-wire serial bus protocol is also possible as in write sequence there is no difference between 3-wire and 4-wire SPI bus protocols.

If the CSB pin is kept always unconnected or high the device can be operated via I2C bus. However, after power-up if the CSB pin is pulled low and there are given clock pulses to the clock input (SCK) this will lock the serial bus to SPI communication. Allowing I2C operation would require switching off the supplies and powering-up the device.

2-WIRE SERIAL DATA INTERFACE (I2C BUS)

I2C Bus Communication and Programmable Alternative I2C Device Address

The I2C bus protocol makes it possible to connect multiple devices on the same bus. The devices are distinguished from each other by unique device addresses. By default, MAS6513 has device address shown in the table 23. The LSB bit (A0) of the device address defines whether the bus is configured to Read (1) or Write (0) operation. In 7-bit address notation the I2C device address is 76_{HEX} (1110110) when the last A0 W/R bit is excluded.

When using SDOFS=11 setting in the Configuration register 1 it is possible to have the device address bit A1 to be defined by the logic state of the SDO pin. Thus, by having external pull-up from the SDO pin to VDDIO selects device address bit A1=1 instead and having the external pull-down to GND selects device address bit A1=0. This allows using two MAS6513 devices on the same I2C bus. See example of such application circuit in figure 11 on page 37.

Additionally, the MAS6513 has programmable I2C bus address located in EEPROM address 17_{HEX}. By default, it has been factory programmed to same as the hard wired address (table 23) i.e. EC_{HEX} (%1110 1100) which corresponds to 76_{HEX} (%1110 110) in 7-bit address notation. After power-up the MAS6513 answers to its default address 76_{HEX} (%1110 110) only but after giving a software reset the MAS6513 answers additionally to device address which has been programmed to the programmable alternative I2C device address in EEPROM. Thus, to take programmable alternative I2C device address feature into use requires having alternative address programmed to EEPROM and giving a software reset after every power-up.

Table 23. MAS6513 default I2C bus device address (76_{HEX})

A7	A6	A5	A4	A3	A2	A1	A0 [W/R]
1	1	1	0	1	1	0	0/1

I2C Bus Protocol Definitions

Data transfer is initiated with a Start bit (S) when SDI is pulled low while SCK stays high. Then, SDI sets the transferred bit while SCK is low and the data is sampled (received) when SCK rises. When the transfer is complete, a Stop bit (P) is sent by releasing the data line to allow it to be pulled up while SCK is constantly high.

Figure 9 shows the start (S) and stop (P) bits and a data bit. Data must be held stable at the SDI pin when SCK is high. Data at the SDI pin can change value only when SCK is low.

Each SDI line byte transfer must contain 8-bits where the most significant bit (MSB) always comes first. Each byte has to be followed by an acknowledge bit (see further below). The number of bytes transmitted per transfer is unrestricted.

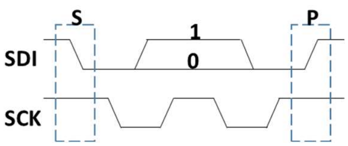


Figure 9. I2C bus protocol definitions

Bus communication includes Acknowledge (A) and not Acknowledge (N) messages. To send an acknowledge the receiver device pulls the SDI low for one SCK clock cycle. For not acknowledge (N) the receiver device leaves the SDI high for one SCK clock cycle in which case the master can then generate either a Stop (P) bit to abort the transfer, or a repeated Start (Sr) bit to start a new transfer.

Abbreviations:
A= Acknowledge by Receiver
N = Not Acknowledge by Receiver
S = Start
Sr = Repeated Start
P = Stop
[grey box] = from Master (MCU) to Slave (MAS6513)
[white box] = from Slave (MAS6513) to Master (MCU)

Measurement Configuration and Start – Write Sequence

Prior starting measurements appropriate configuration setups should be written to the Configuration register 1 (41_{HEX}) and 2 (42_{HEX}). Actual measurements selected by OSRT and OSRC bit settings are started right after receiving measurement setup to the Control register (43_{HEX}).
Table 24 illustrates write of both Configuration registers 1-2 and the Control register in a single write sequence ("burst").
Each serial bus operation, like write, starts with the start (S) bit (see figure 9). After start (S) the MAS6513 device write address (AW) is written to the bus. Next the master writes Configuration 1-2 and Control register data. After each received byte the slave gives an acknowledge (A). Master ends transmission by giving stop (P) command.
Using single write sequence to write into these three registers is possible since their addresses are consecutive and the MAS6513 supports auto increment of the address. In the auto increment function the address is automatically incremented to the next address when either read or write sequence is continued (not ended by a Stop command P) after each read or written data byte.

Table 24. MAS6513 I2C bus burst write sequence of Configuration registers 1-2 and Control register

S	AW	A	ACF1	A	DCF1	A	DCF2	A	DCR	A	P

Abbreviations:
AW = Device write address
AR = Device read address
ACF1 = Configuration register 1 address 41_{HEX}
ACF2 = Configuration register 2 address 42_{HEX}
ACR = Control register address 43_{HEX}
DCF1 = Configuration register 1 data
DCF2 = Configuration register 2 data
DCR = Control register data

Conversion Result – Read Sequence

Table 25 presents a general control sequence for a single data byte Dx read from address Ax.

Table 25. MAS6513 I2C bus single register (address Ax) read sequence bits

S	AW	A	Ax	A	Sr	AR	A	Dx	N	P

Table 26 shows a burst read sequence for reading 24-bit measurement results of both temperature and capacitance. All six result bytes can be read in the same read sequence since temperature and capacitance result register addresses are consecutive and auto increment of address is supported also in read operation.

The read sequence is ended by the Stop bit P only after all the six bytes have been read. The first the three temperature result registers are read in order MSB (DTM), LSB (DTL) and XLSB (DTX) and this is followed by three capacitance result registers in the same order MSB (DCM), LSB (DCL) and XLSB (DCX).

Table 26. MAS6513 I2C bus burst read sequence for six measurement result bytes

S	AW	A	ATR	A	Sr	AR	A	DTM	A	DTL	A	DTX	A	DCM	A	DCL	A	DCX	N	P

Abbreviations:
AW = Device write address
AR = Device read address
ATR = MSB address of Temperature result register; 45_{HEX}
ACR = MSB address of Capacitance result register; 48_{HEX}
Dyx = Conversion result register Data; Temperature (y=T), Capacitance (y=C), MSB (x=M), LSB (x=L) or XLSB (x=X)

Single MAS6513 device on I2C bus

Figure 10 presents application circuit of a single MAS6513 device connected on 2-wire I2C bus. The SDO pin can be optionally configured as an interrupt output by setting SDOFS=01 in the Configuration register 1.

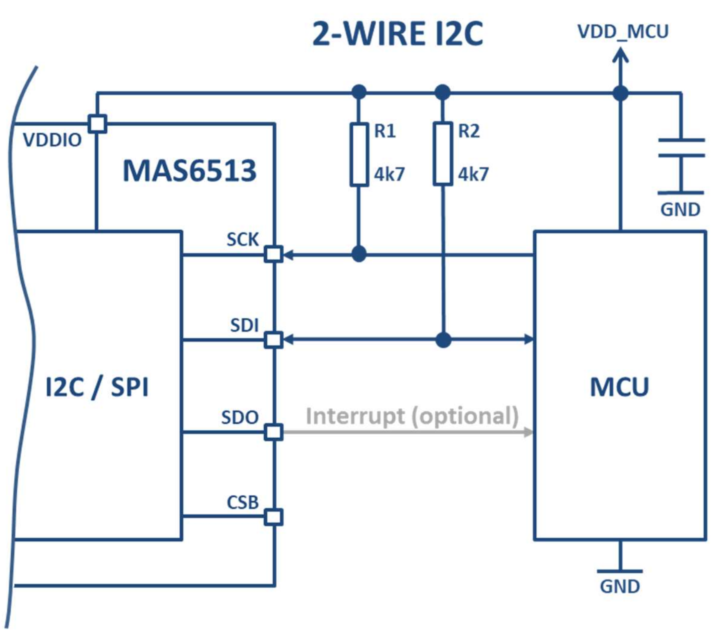


Figure 10. Application circuit of single MAS6513 device connected on the I2C bus

Two MAS6513 devices on the same I2C bus

Figure 11 presents application circuit of two MAS6513 devices connected on the same 2-wire I2C bus. By setting SDOFS=11 in the Configuration register 1 and having additional pull-up (R3) and down (R4) resistors connected to the SDO pins it is possible to have unique I2C bus device addresses in the two MAS6513 devices.

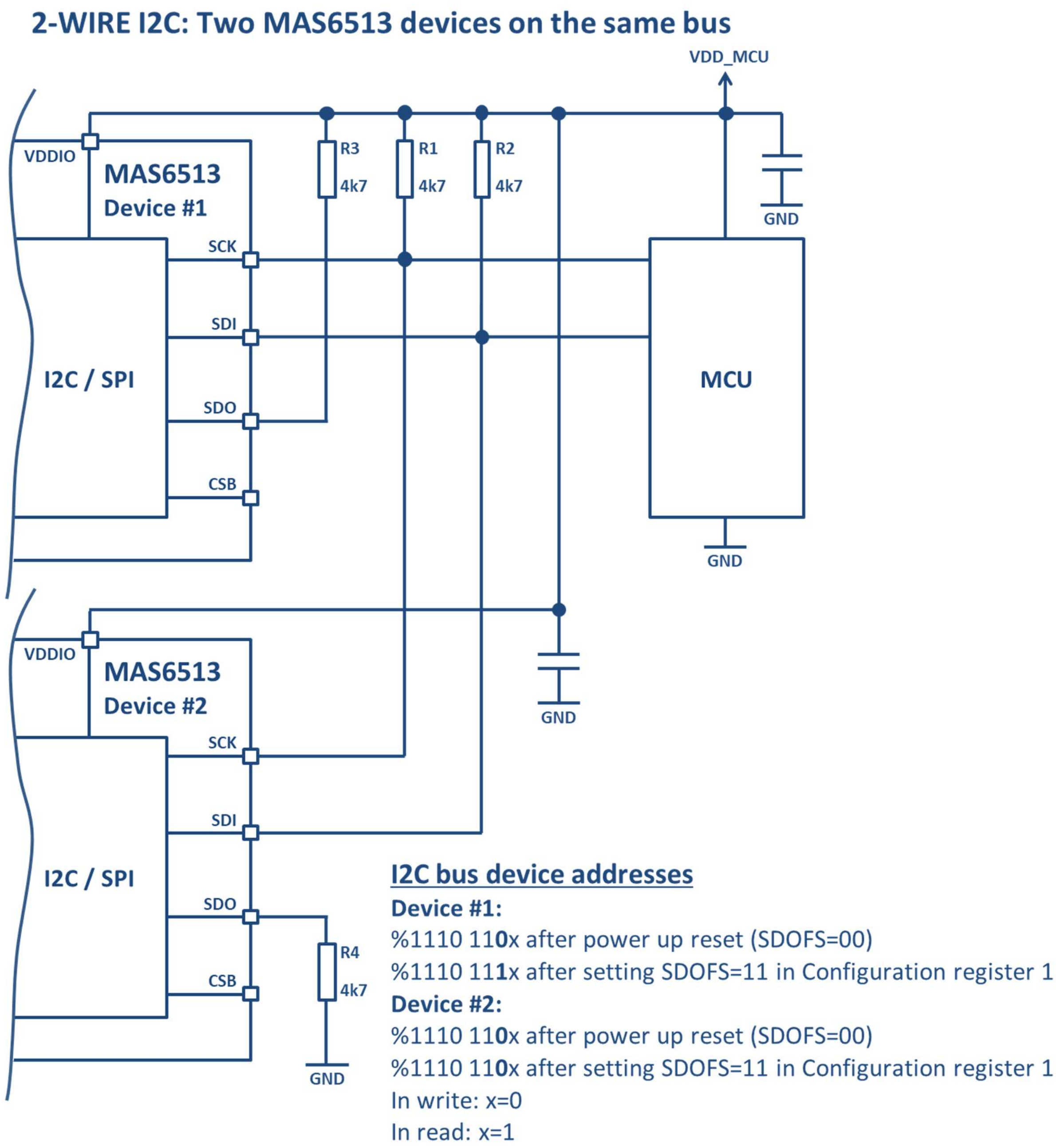


Figure 11. Application circuit of two MAS6513 devices connected on the same I2C bus

4- AND 3-WIRE SERIAL DATA INTERFACE (SPI BUS)

The 4-wire serial SPI bus type interface comprises of serial clock input (SCK), serial data input (SDI), serial data output (SDO) and chip select input (CSB). In 3-wire mode the SDI pin operates as both input and output since it carries bi-directional data transfer.

Selection between 4-wire and 3-wire SPI bus communication is done by the SDOFS bits in the Configuration register 1 (41_{HEX}). By default, the SPI bus is in the 4-wire mode (SDOFS=00). 3-wire mode is available with two different SDO pin functions. The SDOFS=01 selection configures SDO pin as output for interrupts. The SDOFS=10 setting does not have any function. For further details see Configuration register 1 description table 8 on page 20.

In the SPI communication the device selection is done by CSB chip select pin. By setting the CSB pin low activates the SPI bus communication. Note that the CSB pin has internal pull up and to minimize current consumption it should be set low only during SPI communication periods.

Bits are transferred always MSB bit first. This concerns both address and data bits. See figure 12 illustrating 4- wire and 3-wire write access communication (data written to MAS6513).

The data is latched at rising edges of the serial clock (SCK) during which the data input line (SDI) should be kept stable (SPI mode 0 CPOL=CPHA=0 and mode 3 CPOL=CPHA=1). The selection between write or read access is done by MSB address bit (A7) (see EEPROM and register maps in tables 6-7 on page 18). In write access the MSB bit is cleared (A7=0) and in read access it is set (A7=1). The following seven address bits define register address. The address bits are followed by eight data bits.

The MAS6513 has also an auto increment function which means that if there are more than one data byte transferred in read/write by continuing the SCK clocking the additional data bytes are delivered to/from following incremented addresses. The SPI bus data transfer is ended by setting the CSB pin high. In write access communication the MAS6513 keeps the SDO line in high impedance state (HZ) during the whole communication unless interrupt function has been configured to the SDO pin.

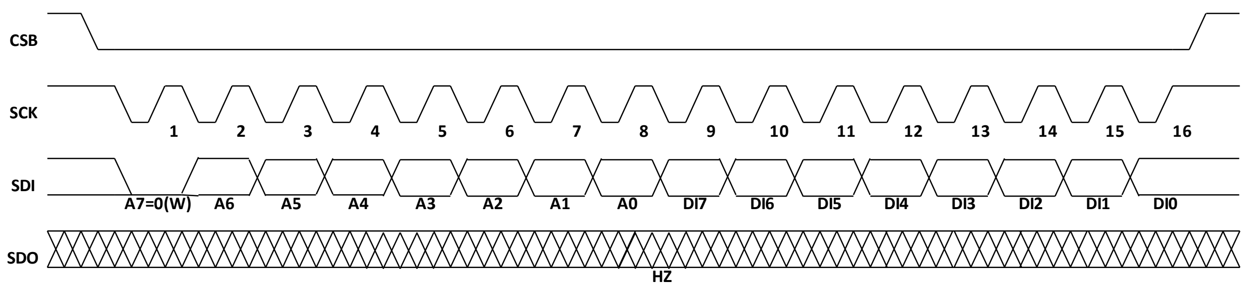


Figure 12. SPI 4-wire (SDOFS=00) and 3-wire (SDOFS=01) protocol – Write access (A7=0)

Figure 13 illustrates 4-wire (SDOFS=00) SPI bus read access communication (A7=1). The SDO line is at high impedance state (HZ) until it outputs the MSB data bit (DO7) at falling edge of the eight SCK clock pulse.

The auto increment function can be utilized also in read access. Thus, if there are more than one data byte read the additional data bytes are delivered from following incremented register addresses.

Returning CSB high ends the SPI communication and sets the SDO pin to high impedance state (HZ).

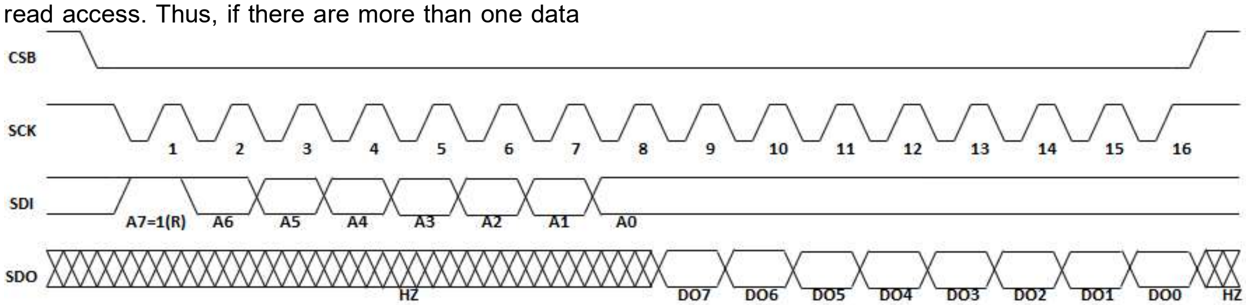


Figure 13. SPI 4-Wire (SDOFS=00) protocol – Read access (A7=1)

Figure 14 illustrates 3-wire (SDOFS=01) SPI bus read access communication. The SDI input line turns into output after falling edge of the eight SCK clock pulse. The first read data bit is the MSB bit and the last LSB bit is send to SDI line at the falling edge of the 15th SCK clock pulse. Master reads the data bits at the rising edges of the SCK clock pulses.

The auto increment function is supported also in 3-wire SPI communication.

In 3-wire SPI bus write access communication the MAS6513 keeps the SDO line in high impedance state (HZ) during the whole communication unless interrupt function has been configured to the SDO pin.

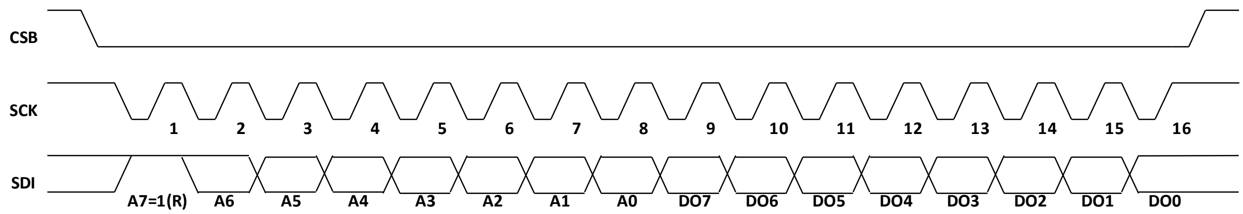


Figure 14. SPI 3-Wire (SDOFS=01) protocol – Read access (A7=1)

CAPACITANCE MEASUREMENT MODES

MAS6513 has three different types of capacitance measurements. Selection between modes is done by CMM bits in the Configuration register 2 (42_{HEX}). See table 9 on page 21. There are two capacitance difference measurement modes available. The CMM=00 selection is suited for changing sensor capacitance from 2pF up to 20pF and the CMM=01 selection is suited changing sensor capacitances from 1pF up to 10pF. Capacitance ratio measurement mode is selected by CMM=10 and capacitance sum mode is by CMM=11.

Capacitance difference mode (CMM=00 or 01)

In the capacitance difference mode, the CDC output result (CODE) is proportional to capacitance difference $\Delta C=(C_S-C_R)$ where the C_S is overall capacitance between CS and CC pins and the C_R is overall capacitance between CR and CC pins. See equation 11.

$$CODE = \frac{CODEFS}{2} \cdot \left[1 + \left(\frac{\Delta C}{C_{REF}}\right) \cdot K_{DIFF}\right] = \frac{CODEFS}{2} \cdot \left[1 + \left(\frac{C_S - C_R}{C_{REF}}\right) \cdot K_{DIFF}\right]$$ **Equation 11.**

CODEFS = 11184810 Full scale output code range

K_{DIFF} = 0.229+0.02*GRDAC (see table 21 for Gain register setting) **Equation 12.**

C_{REF} = 6pF±15% (CMM=00) or 3pF±15% (CMM=01) Internal reference capacitor

$C_S = C_{S\_EXT} + C_{S\_INT}$ External sensor + internal sensor matrix capacitance between CS and CC pins **Equation 13.**

$C_R = C_{R\_EXT} + C_{R\_INT}$ External reference + internal reference matrix capacitance between CR and CC pins **Equation 14.**

$\Delta C_{EXT} = C_{S\_EXT} - C_{R\_EXT}$ Capacitance difference of external capacitances

$\Delta C_{INT} = C_{S\_INT} - C_{R\_INT}$ Capacitance difference of internal offset capacitance matrices **Equation 15.**

$\Delta C = (C_S-C_R) = (C_{S\_EXT} + C_{S\_INT}) - (C_{R\_EXT} + C_{R\_INT}) = \Delta C_{EXT} + \Delta C_{INT}$ **Equation 16.**
Overall capacitance difference

In capacitance difference mode either C_{S_EXT}, C_{R_EXT} or both external capacitances can vary.

Substituting equation 16 to equation 11 lead to equation 17.

$$CODE = \frac{CODEFS}{2} \cdot \left[1 + \left(\frac{\Delta C_{EXT} + \Delta C_{INT}}{C_{REF}}\right) \cdot K_{DIFF}\right]$$ **Equation 17.**

From equations 15 and 17 we see that offset trimming of the CODE is achieved using internal capacitance matrices which define the $\Delta C_{INT} = C_{S\_INT} - C_{R\_INT}$ term. Increasing C_{S_INT} increases CODE and increasing C_{R_INT} decreases CODE. The C_{S_INT} and C_{R_INT} capacitances are adjusted by OCDACS and OCDACR settings respectively (see Internal capacitor matrix registers in tables 19-20). Gain trimming is achieved by gain register GRDAC value (see Gain register in table 21) which adjusts gain coefficient (K_{DIFF}) according to equation 12.

The CDC output result (CODE) ranges from 0 to CODEFS. These correspond to following minimum (ΔC_{EXT_MIN}) and maximum (ΔC_{EXT_MAX}) external input capacitance difference and overall external changing capacitance (ΔC_{EXT_TOT}) values.

$$\Delta C_{EXT\_MIN} = -\frac{C_{REF}}{K_{DIFF}} - \Delta C_{INT}, \ \Delta C_{EXT\_MAX} = \frac{C_{REF}}{K_{DIFF}} - \Delta C_{INT}$$ **Equations 18a, 18b**

$$\Delta C_{EXT\_TOT} = \Delta C_{EXT\_MAX} - \Delta C_{EXT\_MIN} = 2 \cdot \frac{C_{REF}}{K_{DIFF}}$$ **Equations 18c.**

However linear measurement range of CDC is from 10% to 90% of CODEFS. To avoid non-linearity error in the measurements the capacitive front-end should be trimmed to keep the measured external capacitance within the linear measurement range of the CDC. In the linear measurement range the minimum ($\Delta C_{EXT\_LIN\_MIN}$) and maximum ($\Delta C_{EXT\_LIN\_MAX}$) external capacitance difference and overall external changing capacitance ($\Delta C_{EXT\_LIN\_TOT}$) values are as follows.

CAPACITANCE MEASUREMENT MODES (continued)

$$\Delta C_{EXT\_LIN\_MIN} = -80\% \cdot \frac{C_{REF}}{K_{DIFF}} - \Delta C_{INT},\ \Delta C_{EXT\_LIN\_MAX} = 80\% \cdot \frac{C_{REF}}{K_{DIFF}} - \Delta C_{INT}$$ **Equations 19a, 19b.**

$$\Delta C_{EXT\_LIN\_TOT} = \Delta C_{EXT\_LIN\_MAX} - \Delta C_{EXT\_LIN\_MIN} = 1.6 \cdot \frac{C_{REF}}{K_{DIFF}} = 0.8 \cdot \Delta C_{EXT\_TOT}$$ **Equation 19c.**

Example:

CMM=00, GRDAC = 109_{DEC}, OCDACS = 0_{DEC} and OCDACR = 93_{DEC} trim settings correspond to following external input capacitance difference measurement range values.

Capacitance values of offset capacitance matrices:

C_{S_INT} = 22pF*0/255 = 0pF, C_{R_INT} = 22pF*93/255 ≈ 8.03pF, ΔC_{INT} = 0pF - 8.03pF = -8.03pF ⇒

Gain coefficient: K_{DIFF} = 0.229+0.02*109 = 2.409

Overall input range:

ΔC_{EXT_MIN} = -6pF/2.409-(-8.03pF) ≈ 5.54pF

ΔC_{EXT_MAX} = 6pF/2.409-(-8.03pF) ≈ 10.52pF

ΔC_{EXT_TOT} = 2*6pF/2.409 ≈ 4.98pF

Linear input range:

$\Delta C_{EXT\_LIN\_MIN}$ = -0.8*6pF/2.409-(-8.03pF) ≈ 6.04pF

$\Delta C_{EXT\_LIN\_MAX}$ = 0.8*6pF/2.409-(-8.03pF) ≈ 10.02pF

$\Delta C_{EXT\_LIN\_TOT}$ = 0.8*4.98pF ≈ 3.98pF

Note that above calculated values are capacitance difference values between external sensor (CS) and external reference (CR) side capacitances ($\Delta C_{EXT} = C_{S\_EXT} - C_{R\_EXT}$). If there is no external reference capacitor (C_{R_EXT}=0) then these values represent sensor side (CS) capacitance C_{S_EXT} ($\Delta C_{EXT} = C_{S\_EXT} - 0 = C_{S\_EXT}$) minimum and maximum measurement range values. If a fixed external reference capacitor C_{R_EXT} exists then sensor side (CS) capacitance measurement range is C_{R_EXT} added to above ΔC_{EXT} values ($C_{S\_EXT} = \Delta C_{EXT} + C_{R\_EXT}$). If C_{R_EXT} is also varying then above values tell range of C_{S_EXT} and C_{R_EXT} capacitance difference ($\Delta C_{EXT} = C_{S\_EXT} - C_{R\_EXT}$) that can be measured.

Capacitance ratio mode (CMM=10)

In the capacitance ratio mode the CDC output result (CODE) is proportional to capacitance ratio (C_S-C_R)/C_S.

$$CODE = CODEFS \cdot \left[1 - \frac{C_R}{C_S}\right] \cdot K_{RATIO} = CODEFS \cdot \left[1 - \frac{C_{R\_EXT} + C_{R\_INT}}{C_{S\_EXT} + C_{S\_INT}}\right] \cdot K_{RATIO}$$ **Equation 20.**

where

CODEFS = 11184810 Full scale output code range

K_{RATIO} = 193.8/GRDAC (see table 21 for Gain register setting) **Equation 21.**

$C_S = C_{S\_EXT} + C_{S\_INT}$ External sensor + internal sensor matrix capacitance between CS and CC pins
$C_R = C_{R\_EXT} + C_{R\_INT}$ External reference + internal reference matrix capacitance between CR and CC pins

CAPACITANCE MEASUREMENT MODES (continued)

Capacitance sum mode (CMM=11)

In the capacitance difference mode, the CDC output result (CODE) is proportional to sum of external sensor capacitances (C_{S_EXT}+C_{R_EXT}) where the C_{S_EXT} is sensor capacitance between CS and CC pins and the C_{R_EXT} is sensor capacitance between CR and CC pins. Signal offset adjustment is accomplished by sum of internal capacitance matrix capacitances (C_{S_INT}+C_{R_INT}). The resulted output code dependency is shown in equation 22.

$$CODE = \frac{CODEFS}{2} \cdot \left[1 + \left(\frac{C_{S\_EXT} + C_{R\_EXT} - C_{S\_INT} - C_{R\_INT}}{C_{REF}}\right) \cdot K_{SUM}\right]$$ **Equation 22.**

where

CODEFS = 11184810 Full scale output code range

K_{SUM} = 0.229+0.02*GRDAC (see table 21 for Gain register setting) **Equation 23.**

C_{REF} = 6pF ±15% Internal reference capacitor

ΣC_{EXT} = C_{S_EXT} + C_{R_EXT} Sum of external sensor capacitances **Equation 24a.**

ΣC_{INT} = C_{S_INT} + C_{R_INT} Sum of internal offset capacitors **Equation 24b.**

In capacitance sum mode either C_{S_EXT} or C_{R_EXT} or both external capacitances can vary.

Substituting equations 24a and 24b to equation 22 lead to equation .

$$CODE = \frac{CODEFS}{2} \cdot \left[1 + \left(\frac{\Sigma C_{EXT} - \Sigma C_{INT}}{C_{REF}}\right) \cdot K_{SUM}\right]$$ **Equation 25.**

From equations 24b and 25 we see that offset trimming of the CODE is achieved using internal capacitance matrices which define the ΣC_{INT} = C_{S_INT} + C_{R_INT} term. Increasing C_{S_INT} and C_{R_INT} decreases CODE and decreasing C_{S_INT} and C_{R_INT} increases CODE. The C_{S_INT} and C_{R_INT} capacitances are adjusted by OCDACS and OCDACR settings respectively (see Internal capacitor matrix registers in tables 19-20). Gain trimming is achieved by gain register GRDAC value (see Gain register in table 21) which adjusts gain coefficient (K_{SUM}) according to equation 23.

The CDC output result (CODE) ranges from 0 to CODEFS. These correspond to following minimum (ΣC_{EXT_MIN}) and maximum (ΣC_{EXT_MAX}) external input capacitance sum and overall external changing capacitance ($\Delta\Sigma C_{EXT\_TOT}$) values.

$$\Sigma C_{EXT\_MIN} = -\frac{C_{REF}}{K_{SUM}} + \Sigma C_{INT},\ \Sigma C_{EXT\_MAX} = \frac{C_{REF}}{K_{SUM}} + \Sigma C_{INT}$$ **Equations 26a, 26b**

$$\Delta\Sigma C_{EXT\_TOT} = \Sigma C_{EXT\_MAX} - \Sigma C_{EXT\_MIN} = 2 \cdot \frac{C_{REF}}{K_{SUM}}$$ **Equations 26c.**

However linear measurement range of CDC is from 10% to 90% of CODEFS. To avoid non-linearity error in the measurements the capacitive front-end should be trimmed to keep the measured external capacitance within the linear measurement range of the CDC. In the linear measurement range the minimum ($\Sigma C_{EXT\_LIN\_MIN}$) and maximum ($\Sigma C_{EXT\_LIN\_MAX}$) external capacitance sum and overall external changing capacitance ($\Delta\Sigma C_{EXT\_LIN\_TOT}$) values are as follows.

$$\Sigma C_{EXT\_LIN\_MIN} = -80\% \cdot \frac{C_{REF}}{K_{SUM}} - \Sigma C_{INT},\ \Sigma C_{EXT\_LIN\_MAX} = 80\% \cdot \frac{C_{REF}}{K_{SUM}} - \Sigma C_{INT}$$ **Equations 27a, 27b.**

$$\Delta\Sigma C_{EXT\_LIN\_TOT} = \Sigma C_{EXT\_LIN\_MAX} - \Sigma C_{EXT\_LIN\_MIN} = 1.6 \cdot \frac{C_{REF}}{K_{SUM}} = 0.8 \cdot \Delta\Sigma C_{EXT\_TOT}$$ **Equation 27c.**

MAS6513 in capacitance difference mode

Optimal trim settings which adjust capacitive signal to linear conversion range 10%...90% of the CDC are calculated as follows. At first offset C_{OFS_EXT} of external capacitance ranges C_{S_EXT} and C_{R_EXT} is calculated.

$C_{OFS\_EXT} = (\Delta C_{EXT\_MIN} + \Delta C_{EXT\_MAX}) / 2 =$

$= (C_{S\_EXT\_MIN} - C_{R\_EXT\_MAX} + C_{S\_EXT\_MAX} - C_{R\_EXT\_MIN}) / 2$ **Equation 28.**

The offset compensated to zero by using either C_{S_INT} or C_{R_INT} capacitor matrices depending on the offset polarity.

If $C_{OFS\_EXT} \geq 0pF$

then $C_{R\_INT} = C_{OFS\_EXT}$ and $C_{S\_INT} = 0pF$

else $C_{R\_INT} = 0pF$ and $C_{S\_INT} = -C_{OFS\_EXT}$

Corresponding capacitance matrix register values (decimal) are calculated as follows.

$REG_{7CHEX} = OCDACS = (C_{S\_INT}/22pF)*255_{DEC}$ **Equation 29.**

$REG_{7DHEX} = OCDACR = (C_{R\_INT}/22pF)*255_{DEC}$ **Equation 30.**

Optimal gain coefficient (K_{DIFF}) value scales capacitive signal to linear conversion range 10%...90% of the CDC and it is calculated as follows.

$K_{DIFF} = 1.6*C_{REF} / (\Delta C_{EXT\_MAX} - \Delta C_{EXT\_MIN}) =$

$= 1.6*C_{REF} / (C_{S\_EXT\_MAX} - C_{S\_EXT\_MIN} + C_{R\_EXT\_MAX} - C_{R\_EXT\_MIN})$ **Equation 31.**

where $C_{REF} = 6pF \pm 15\%$.

Corresponding Gain register (REG_{E5HEX}) value (decimal) can be solved from the equation 12 presented on page 40 as follows.

$REG_{E5HEX} = GRDAC = (K_{DIFF}-0.229)/0.02$ **Equation 32.**

Example 1: No external reference capacitor C_{R_EXT}

$C_{S\_EXT\_MIN} = 8pF$ and $C_{R\_EXT\_MAX} = 0pF$ at sensed parameter (pressure, humidity etc.) minimum
$C_{S\_EXT\_MAX} = 12pF$ and $C_{R\_EXT\_MIN} = 0pF$ at sensed parameter (pressure, humidity etc.) maximum ⇒
$C_{R\_OFS\_EXT} = (8pF-0pF+12pF-0pF)/2=10pF$
$C_{OFS\_EXT} \geq 0$ ⇒
$C_{R\_INT} = C_{OFS\_EXT} = 10pF$ and $C_{S\_INT} = 0$ pF
$K_{DIFF} = 1.6*6pF/(12pF-8pF+0pF-0pF) = 2.4$ ⇒
REG_{7CHEX} = OCDACS = (0pF/22pF)*255 = **0_{DEC} (CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (10pF/22pF)*255 = 115.91 ≈ **116_{DEC} (CR capacitor matrix)**
REG_{7EHEX} = GRDAC = (2.4-0.229)/0.02 = 108.55 ≈ **109_{DEC} (Gain register)**

Example 2: Both C_{S_EXT} and C_{R_EXT} vary but to opposite directions

$C_{S\_EXT\_MIN} = 10pF$ and $C_{R\_EXT\_MAX} = 14.5pF$ at sensed parameter (pressure, humidity etc.) minimum
$C_{S\_EXT\_MAX} = 14pF$ and $C_{R\_EXT\_MIN} = 10pF$ at sensed parameter (pressure, humidity etc.) maximum ⇒
$C_{OFS\_EXT} = (10pF-14.5pF+14pF-10pF)/2 = -0.25pF$
$C_{OFS\_EXT} < 0$ ⇒
$C_{R\_INT} = 0pF$ and $C_{S\_INT} = -C_{OFS\_EXT} = 0.25pF$
$K_{DIFF} = 1.6*6pF/(14pF-10pF+14.5pF-10pF) = 1.129$ ⇒
REG_{7CHEX} = OCDACS = (0.25pF/22pF)*255 = 2.90 ≈ **3_{DEC} (CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (0pF/22pF)*255 = **0_{DEC} (CR capacitor matrix)**
REG_{7EHEX} = GRDAC = (1.129-0.229)/0.02 = 45.00 ≈ **45_{DEC} (Gain register)**

The found REG_{7CHEX}, REG_{7DHEX} and REG_{7EHEX} trim register values need to be stored to corresponding non-volatile EEPROM addresses. In I2C and SPI write communication these are $3C_{HEX}$, $3D_{HEX}$ and $3E_{HEX}$. See EEPROM map table 6 on page 18.

TRIMMING FOR SENSOR CAPACITANCE (continued)

MAS6513 in capacitance ratio mode

Optimal trim settings which adjust capacitive signal to linear conversion range 10%...90% of the CDC are found as follows.

$C_{OFS} = [0.9*C_{S\_EXT\_MAX}*(C_{S\_EXT\_MIN} – C_{R\_EXT\_MAX}) – 0.1*C_{S\_EXT\_MIN}*(C_{S\_EXT\_MAX} - C_{R\_EXT\_MIN})]$ /
$[0.9*C_{S\_EXT\_MAX} - 0.1*C_{S\_EXT\_MIN}]$ **Equation 33.**

If $C_{OFS} \geq 0pF$

then $C_{R\_INT} = C_{OFS}$ and $C_{S\_INT} = 0pF$

else $C_{R\_INT} = 0pF$ and C_{S_INT} is calculated as follows.

$a = 0.8$
$b = 0.9*(C_{S\_EXT\_MAX} + C_{S\_EXT\_MIN} – C_{R\_EXT\_MAX}) – 0.1*(C_{S\_EXT\_MAX} + C_{S\_EXT\_MIN} - C_{R\_EXT\_MIN})$ **Equation 34a.**
$c = 0.9*C_{S\_EXT\_MAX}*(C_{S\_EXT\_MIN} – C_{R\_EXT\_MAX}) – 0.1*C_{S\_EXT\_MIN}*(C_{S\_EXT\_MAX} - C_{R\_EXT\_MIN})$ **Equation 34b.**
$C_{S\_INT1} = [-b+\sqrt{(b^2-4*a*c)}]/2/a$ **Equation 34c.**
$C_{S\_INT2} = [-b-\sqrt{(b^2-4*a*c)}]/2/a$ **Equation 34d.**

If $C_{S\_INT1} \geq 0pF$ then $C_{S\_INT} = C_{S\_INT1}$ else $C_{S\_INT} = C_{S\_INT2}$

If C_{R_EXT} does not exist ($C_{R\_EXT} = 0pF$) the equation 33 simplifies to following form.

$C_{OFS} = C_{R\_INT} = 0.8*C_{S\_EXT\_MAX}*C_{S\_EXT\_MIN} / (0.9*C_{S\_EXT\_MAX} - 0.1*C_{S\_EXT\_MIN})$ **Equation 35.**

Corresponding capacitance matrix register (REG_{E3HEX} and REG_{E4HEX}) values (decimal) are calculated using equations 2 and 3 presented on page 29.

Optimal gain coefficient (K_{RATIO}) value is calculated as follows.

$K_{RATIO} = 0.1 * (C_{S\_EXT\_MIN} + C_{S\_INT}) / (C_{S\_EXT\_MIN} + C_{S\_INT} – C_{R\_EXT\_MAX} - C_{R\_INT}) =$ **Equation 36a.**
$= 0.9 * (C_{S\_EXT\_MAX} + C_{S\_INT}) / (C_{S\_EXT\_MAX} + C_{S\_INT} – C_{R\_EXT\_MIN} - C_{R\_INT})$ **Equation 36b.**

Corresponding Gain register (REG_{E5HEX}) value (decimal) can be solved from the equation 21 presented on page 41 as follows.

$GRDAC = 193.8/ K_{RATIO}$ (see table 21 for Gain register setting) **Equation 37.**

Example 1: Only C_{S_EXT} varies and C_{R_EXT} does not exist ($C_{R\_EXT} = 0pF$)

$C_{S\_EXT\_MIN}$=4pF at sensed parameter (pressure, humidity etc.) minimum
$C_{S\_EXT\_MAX}$=12pF at sensed parameter (pressure, humidity etc.) maximum
$C_{R\_EXT\_MIN/MAX} = 0pF$ (no external reference capacitor) $\Rightarrow$

$C_{OFS} = 0.8*12pF*4pF/(0.9*12pF-0.1*4pF) = 3.69pF \geq 0$ $\Rightarrow$
$C_{R\_INT} = C_{OFS} = 3.69pF$ and $C_{S\_INT} = 0pF$
$K_{RATIO} = 0.1*(4pF+0pF)/(4pF-0pF-0pF-3.69pF) = 1.3$

REG_{7CHEX} = OCDACS = (0pF/22pF)*255 = **0_{DEC} (CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (3.69pF/22pF)*255 ≈ **43_{DEC} (CR capacitor matrix)**
REG_{7EHEX} = GRDAC = 193.8/1.3 = 149.08 ≈ **149_{DEC} (Gain register)**

The found REG_{7CHEX}, REG_{7DHEX} and REG_{7EHEX} trim register values need to be stored to corresponding non-volatile EEPROM addresses. In I2C and SPI write communication these are $3C_{HEX}$, $3D_{HEX}$ and $3E_{HEX}$. See EEPROM map table 6 on page 18.

TRIMMING FOR SENSOR CAPACITANCE (continued)

Example 2: Only C_{S_EXT} varies but fixed C_{R_EXT} exists

$C_{S\_EXT\_MIN}$=9pF and $C_{R\_EXT\_MAX}$=10pF at sensed parameter (pressure, humidity etc.) minimum
$C_{S\_EXT\_MAX}$=14pF and $C_{R\_EXT\_MIN}$=10pF at sensed parameter (pressure, humidity etc.) maximum ⇒

C_{OFS} = [0.9*14pF*(9pF-10pF)-0.1*9pF*(14pF-10pF)]/(0.9*14pF-0.1*9pF)= -1.38pF < 0 ⇒
C_{R_INT} = 0pF
a = 0.8
b = 0.9*(14pF+9pF-10pF)-0.1*(14pF+9pF-10pF)= 10.4pF
c = 0.9*14pF*(9pF-10pF)-0.1*9pF*(14pF-10pF)= -16.2 pF^2
C_{S_INT1} = {-10.4pF+√ [(10.4pF)^2-4*0.8*(-16.2)pF^2]}/2/0.8= 1.406pF
C_{S_INT2} = {-10.4pF-√ [(10.4pF)^2-4*0.8*(-16.2)pF^2]}/2/0.8= -14.406pF ⇒
C_{S_INT} = 1.406pF
K_{RATIO} = 0.1*(9pF+1.406pF)/(9pF+1.406pF-10pF-0pF) = 2.563

REG_{7CHEX} = OCDACS = (1.406pF/22pF)*255 = 16.29 ≈ **16_{DEC} (CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (0pF/22pF)*255 = **0_{DEC} (CR capacitor matrix)**
REG_{7EHEX} = GRDAC = 193.8/2.563 = 75.61 ≈ **76_{DEC} (Gain register)**

Example 3: Both C_{S_EXT} and C_{R_EXT} vary but to opposite directions

$C_{S\_EXT\_MIN}$=10pF and $C_{R\_EXT\_MAX}$=14.5pF at sensed parameter (pressure, humidity etc.) minimum
$C_{S\_EXT\_MAX}$=14pF and $C_{R\_EXT\_MIN}$=10pF at sensed parameter (pressure, humidity etc.) maximum ⇒

C_{OFS} = [0.9*14pF*(10pF-14.5pF)-0.1*10pF*(14pF-10pF)]/(0.9*14pF-0.1*10pF) = -5.23pF < 0 ⇒
C_{R_INT} = 0pF
a = 0.8
b = 0.9*(14pF+10pF-14.5pF)-0.1*(14pF+10pF-10pF) = 7.15pF
c = 0.9*14pF*(10pF-14.5pF)-0.1*10pF*(14pF-10pF) = -60.7 pF^2
C_{S_INT1} = {-7.15pF+√ [(7.15pF)^2-4*0.8*(-60.7)pF^2]}/2/0.8 = 5.321pF
C_{S_INT2} = {-7.15pF-√ [(7.15pF)^2-4*0.8*(-60.7)pF^2]}/2/0.8 = -14.259pF ⇒
C_{S_INT} = 5.321pF
K_{RATIO} = 0.1*(10pF+5.321pF)/(10pF+5.321pF-14.5pF-0pF) = 1.866

REG_{7CHEX} = OCDACS = (5.321pF/22pF)*255 = 61.68 ≈ **62_{DEC} (CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (0pF/22pF)*255 = **0_{DEC} (CR capacitor matrix)**
REG_{7EHEX} = GRDAC = 193.8/1.866 = 103.86 ≈ **104_{DEC} (Gain register)**

The found REG_{7CHEX}, REG_{7DHEX} and REG_{7EHEX} trim register values need to be stored to corresponding non-volatile EEPROM addresses. In I2C and SPI write communication these are $3C_{HEX}$, $3D_{HEX}$ and $3E_{HEX}$. See EEPROM map table 6 on page 18.

TRIMMING FOR SENSOR CAPACITANCE (continued)

MAS6513 in capacitance sum mode

Optimal trim settings which adjust capacitive signal to linear conversion range 10%...90% of the CDC are calculated as follows. At first offset C_{OFS_EXT} of external capacitance ranges C_{S_EXT} and C_{R_EXT} is calculated.

$C_{OFS\_EXT} = (\Sigma C_{EXT\_MIN} + \Sigma C_{EXT\_MAX}) / 2 =$

$= (C_{S\_EXT\_MIN} + C_{S\_EXT\_MAX} + C_{R\_EXT\_MAX} + C_{R\_EXT\_MIN}) / 2$ **Equation 38.**

Offset is compensated by sum of internal capacitor matrices C_{S_INT} and C_{R_INT}. We can choose both matrices to compensate same amount of offset capacitance.

$C_{S\_INT} = C_{R\_INT} = C_{OFS\_EXT} / 2$ **Equation 39.**

Corresponding capacitance matrix register values (decimal) are calculated as follows.

$REG_{7CHEX} = OCDACS = (C_{S\_INT}/22pF)*255_{\mathbf{DEC}}$ **Equation 40a.**

$REG_{7DHEX} = OCDACR = (C_{R\_INT}/22pF)*255_{\mathbf{DEC}}$ **Equation 40b.**

Optimal gain coefficient (K_{SUM}) value scales capacitive signal to linear conversion range 10%...90% of the CDC and it is calculated as follows.

$K_{SUM} = 1.6*C_{REF} / (\Sigma C_{EXT\_MAX} - \Sigma C_{EXT\_MIN})$ **Equation 41.**

where $C_{REF} = 6pF \pm 15\%$.

Corresponding Gain register (REG_{E5HEX}) value (decimal) can be solved from the equation 23 presented on page 42 as follows.

$REG_{7EHEX} = GRDAC = (K_{SUM}-0.229)/0.02$ **Equation 42.**

Example 1: Both C_{S_EXT} and C_{R_EXT} vary to same directions

$C_{S\_EXT\_MIN} = 10pF$ and $C_{R\_EXT\_MIN} = 10pF$ at sensed parameter minimum
$C_{S\_EXT\_MAX} = 14pF$ and $C_{R\_EXT\_MAX} = 14.5pF$ at sensed parameter maximum $\Rightarrow$
$C_{OFS\_EXT} = (10pF+14.5pF+14pF+10pF)/2 = 24.25pF$
Note that since sum capacitances up to 10pF+14.5pF=24.5pF exist which is >20pF there has to be used clock division by 2 option.
$C_{S\_INT} = C_{R\_INT} = C_{OFS\_EXT} / 2 = 24.25pF / 2 = 12.125pF$
$K_{SUM} = 1.6*6pF/((14.5pF+14pF)-(10pF+10pF)) = 1.129$ $\Rightarrow$
REG_{7CHEX} = OCDACS = (12.25pF/22pF)*255 = $141_{\mathbf{DEC}}$ **(CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (12.25F/22pF)*255 = $141_{\mathbf{DEC}}$ **(CS capacitor matrix)**
REG_{7EHEX} = GRDAC = (1.129-0.229)/0.02 = 45.00 ≈ **45_{DEC} (Gain register)**

Example 2: Both C_{S_EXT} and C_{R_EXT} vary but to opposite directions

$C_{S\_EXT\_MIN} = 10pF$ and $C_{R\_EXT\_MAX} = 15.5pF$ at sensed parameter minimum
$C_{S\_EXT\_MAX} = 15pF$ and $C_{R\_EXT\_MIN} = 11pF$ at sensed parameter maximum $\Rightarrow$
$C_{OFS\_EXT} = (10pF+15.5pF+15pF+11pF)/2 = 25.75pF$
Note that since sum capacitances up to 11pF+15.5pF=26.5pF exist which is >20pF there has to be used clock division by 2 option.
$C_{S\_INT} = C_{R\_INT} = C_{OFS\_EXT} / 2 = 25.75pF / 2 = 12.88pF$
$K_{SUM} = 1.6*6pF/((15.5pF+11pF)-(15pF+10pF)) = 6.4$ $\Rightarrow$
REG_{7CHEX} = OCDACS = (12.88pF/22pF)*255 = $149_{\mathbf{DEC}}$ **(CS capacitor matrix)**
REG_{7DHEX} = OCDACR = (12.88F/22pF)*255 = $149_{\mathbf{DEC}}$ **(CS capacitor matrix)**
REG_{7EHEX} = GRDAC = (6.4-0.229)/0.02 = 308.55 >255 $\Rightarrow$ GRDAC = $255_{\mathbf{DEC}}$ **(Gain register)**

The found REG_{7CHEX}, REG_{7DHEX} and REG_{7EHEX} trim register values need to be stored to corresponding non-volatile EEPROM addresses. In I2C and SPI write communication these are $3C_{HEX}$, $3D_{HEX}$ and $3E_{HEX}$. See EEPROM map table 6 on page 18.

TEMPERATURE MEASUREMENT

The MAS6513 has an internal temperature sensor for temperature measurement. The temperature sensor output is proportional to absolute temperature (PTAT). Temperature information is needed for temperature indication and temperature compensation of sensor signal.

The temperature measurement is started by writing temperature measurement setup (OSRT<>000 and MODE<>00) to the Control register ($C3/43_{HEX}$). Typically, already a low over sampling ratio (OSRT) selection 2x offers sufficient resolution for the temperature measurement.

The internal temperature sensor has offset and gain variation and small non-linearity (see ELECTRICAL CHARACTERISTICS table). Depending on temperature measurement accuracy requirement the offset, gain and non-linearity of PTAT sensor can be corrected by applying appropriate calibration coefficients and enabling calibrated value calculation (XCALC=0).
In low precision the offset and gain calibration is sufficient (2nd order calibration coefficient is set to zero) but in high precision the second order non-linearity calibration should be included.

Linear temperature sensor model

The linear model of temperature sensor A/D conversion result (CODE) as function of temperature (T) is presented in equation 43.

$CODE = a + b \cdot T$ **Equation 43.**

Typical model parameters for Celsius scale (°C) temperature are as follows.
a=3753812 count
b=42541 count/°C

The linear model calculating temperature (T) from A/D conversion result of temperature (CODE) is presented in equation 44.

$T = a + b \cdot CODE$ **Equation 44.**

Typical model parameters for Celsius scale (°C) output temperature are as follows.

a= -88.23 °C	PTAT temperature sensor offset
b= 2.35058E-05 °C/count	PTAT temperature sensor slope

2nd order temperature sensor model

The non-linear model of temperature sensor A/D conversion result (CODE) as function of temperature (T) is presented in equation 45.

$CODE = a + b \cdot T + c \cdot T^2$ **Equation 45.**

Typical model parameters for Celsius scale (°C) temperature are as follows.
a=3750776 count
b=42015 count/°C
c=6.17287 count/°C^2

The non-linear model calculating temperature (T) from A/D conversion result of temperature (CODE) is presented in equation 46.

$T = a + b \cdot CODE + c \cdot CODE^2$ **Equation 46.**

Typical model parameters for Celsius scale (°C) output temperature are as follows.

a= -90.40 °C	PTAT temperature sensor offset
b= 2.44008E-05 °C/count	PTAT temperature sensor slope
c= -8.01412E-14 °C/count^2	PTAT temperature sensor non-linearity

Note that above model parameters are subject to process variations. See more details of internal PTAT temperature sensor variations in the ELECTRICAL CHARACTERISTICS table on page 4.

APPLICATION INFORMATION

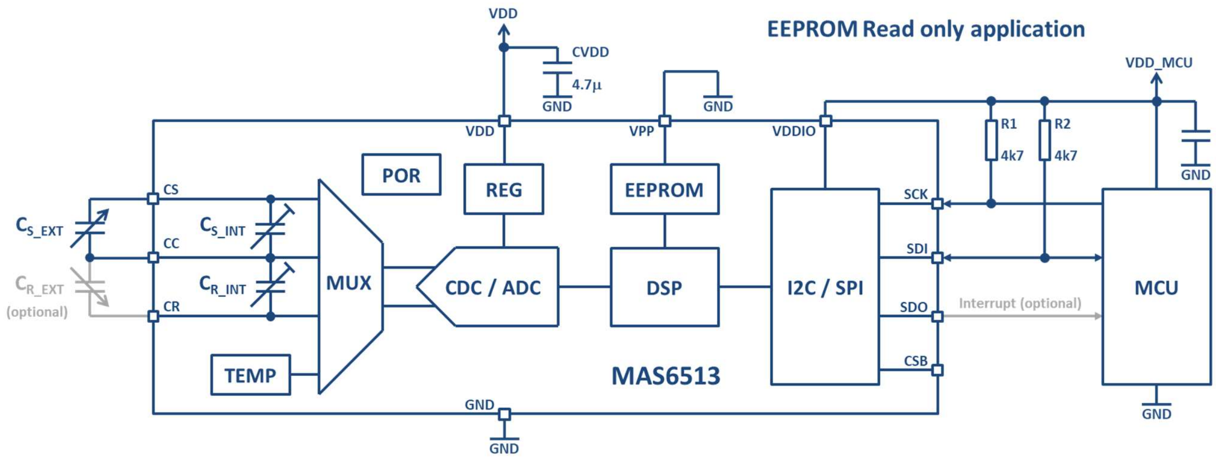


Figure 15. MAS6513 EEPROM read only application using I2C bus communication

Figure 15 presents typical MAS6513 end application circuit using 2-wire I2C bus. The EEPROM is read only and protected from write by having EEPROM programming voltage pin (VPP) connected to ground (GND).

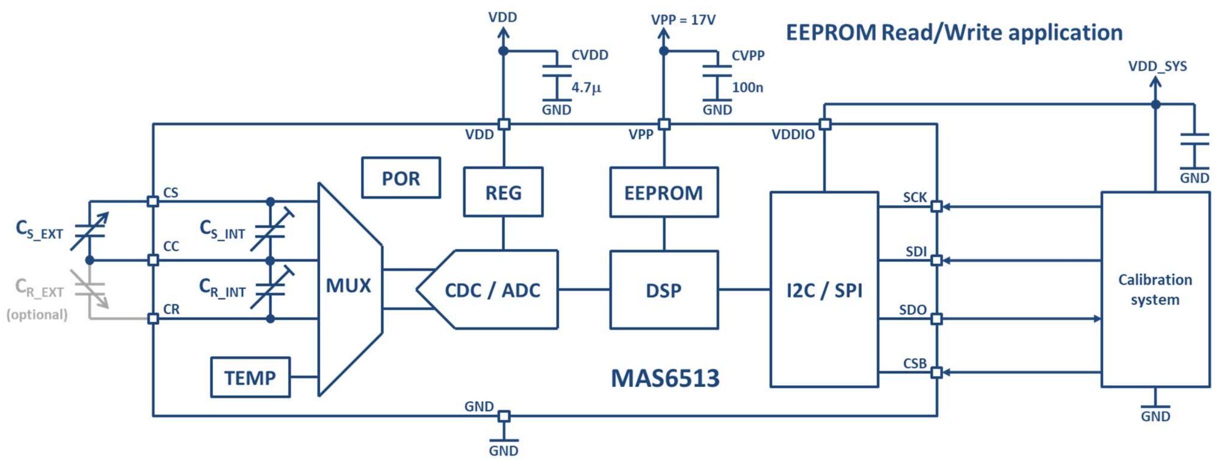


Figure 16. MAS6513 EEPROM read/write application using 4-wire SPI bus communication

Figure 16 presents typical MAS6513 calibration system circuit using 4-wire SPI bus communication. The EEPROM has both write and read capability when having the 17V voltage applied to the EEPROM programming voltage pin (VPP). This enables writing trimming, calibration coefficient and other data to the non-volatile EEPROM memory.

APPLICATION INFORMATION (continued)

IIR filter step response and noise filtering

Digital first order IIR low pass filter can be used to damp sudden variations in the sensor signal and to reduce noise. There are eight filter coefficients (COEFF) selectable from 1 up to 128 by the FILTER setting in the Configuration register 2. The COEFF=1 setting corresponds to no filtering and the filter is bypassed. The larger coefficient the narrower filter band-width and the longer step response. Table 27 presents noise scaling factors and step responses at the different IIR filtering options. However, note that the step response to the first measurement result is immediate since the first result ($CODE_{ADC}$) is considered also as previous filtered output ($CODE_{OLD}$) in the filter equation 1 on page 21. See also figure 17 illustrating sensor signal step responses at different filter coefficients.

Filter band-width (BW) depends on both filter coefficient (COEFF) and measurement repeat rate i.e. sampling rate (fs). See equation 47 and table 27 presenting filter band-width factor K=BW/fs at different filter coefficient values which is needed in the filter band-width calculation.

Table 27. IIR filter band-width and noise scale factors and step response samples

COEFF	Noise scale factor	Samples to reach ≥75% of step response	Samples to reach ≥90% of step response	Filter 3dB band-width factor K
[-]	[-]	[pcs]	[pcs]	[-]
1 (no filtering)	1	1	1	-
2	0.58	2	4	9.06
4	0.38	5	9	21.84
8	0.26	11	18	47.05
16	0.18	22	36	97.36
32	0.13	44	73	197.9
64	0.09	89	147	398.97
128	0.07	177	294	801.1

$BW = f_s / K$ **Equation 47.**

For example, IIR filter band-width at fs=10Hz measurement rate and COEFF=8 setting is BW = 10Hz / 47.05 = 0.213Hz. 90% step response takes 18 samples i.e. 18/10Hz=1.8 seconds and noise level is reduced to about quarter (0.26x) when compared to noise without filtering.

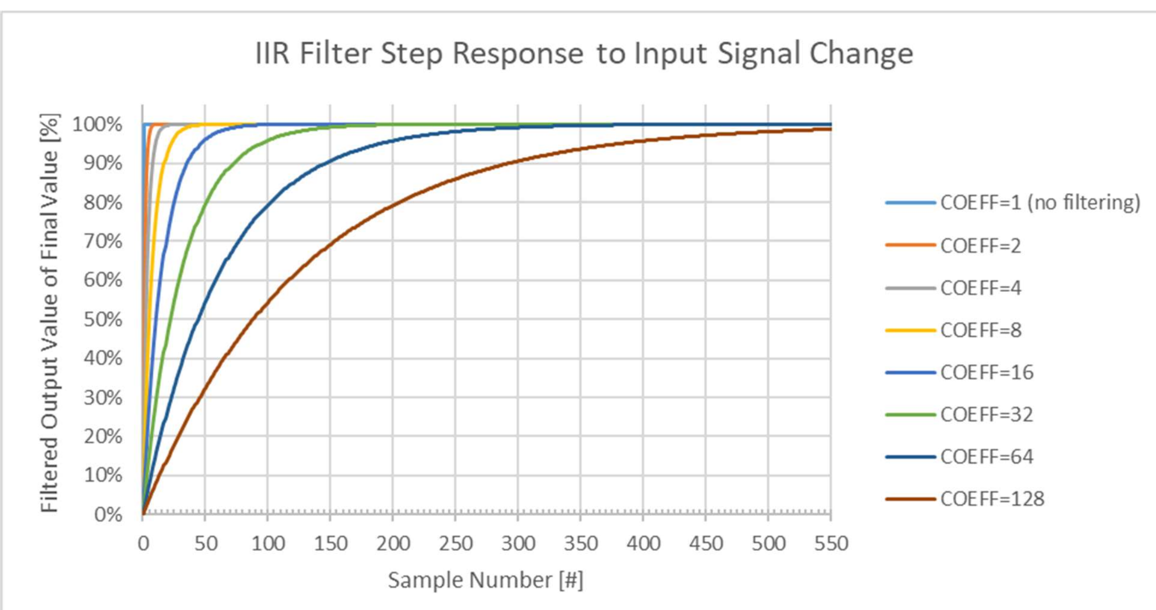
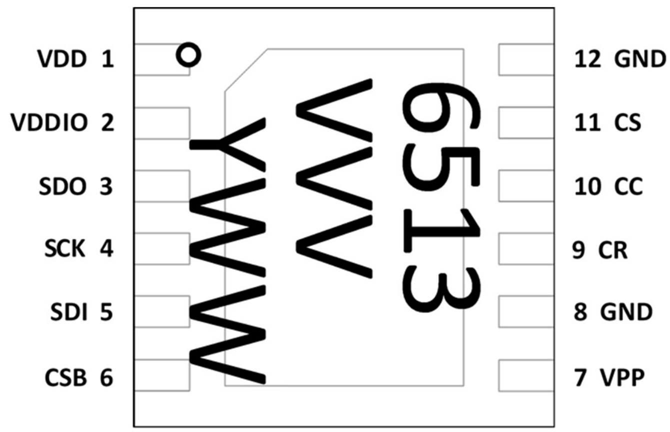


Figure 17. IIR filter step response to input signal change

MAS6513 IN DFN-12 3x3x0.75 PACKAGE (SAMPLES ONLY)



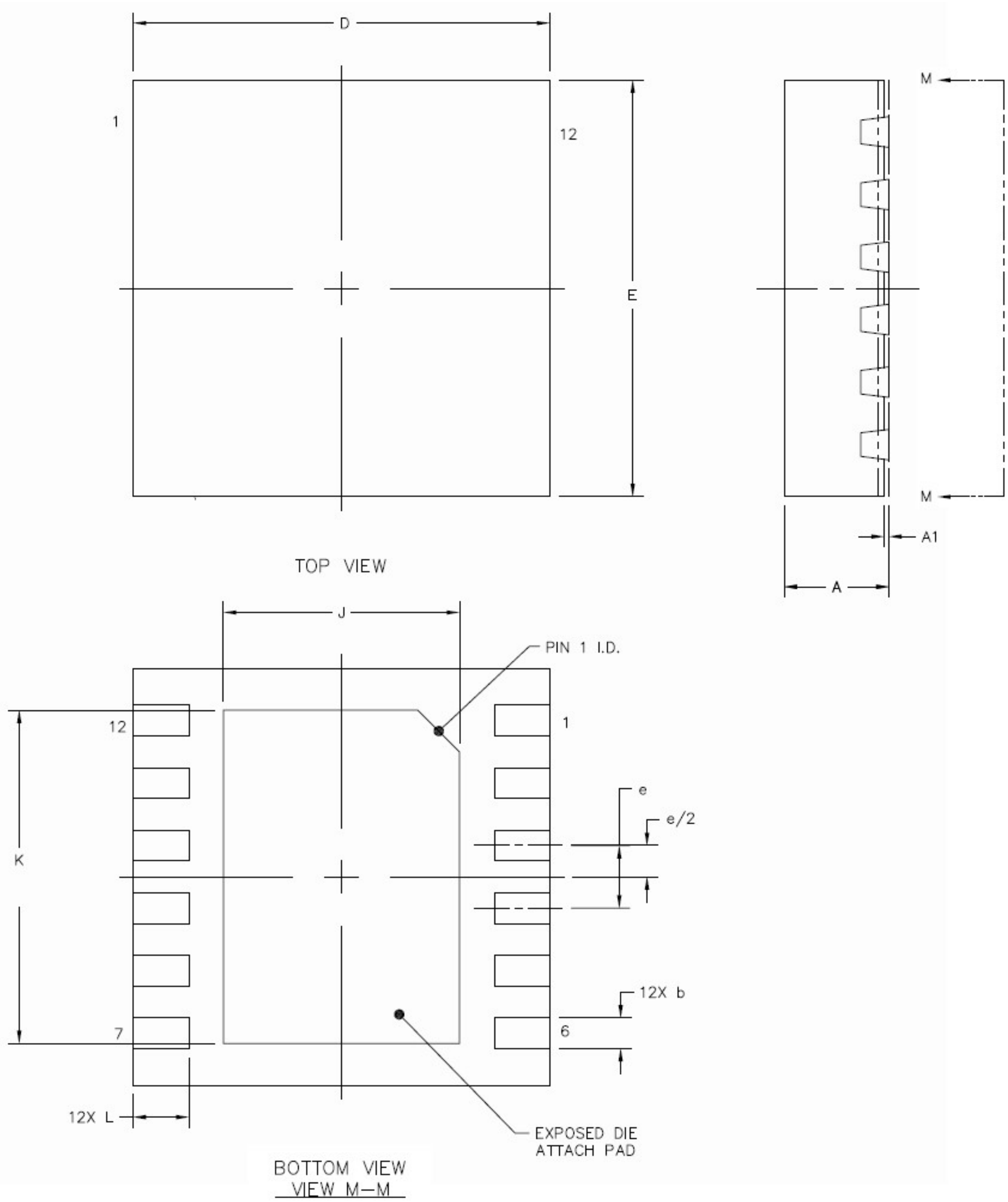
Top Marking Information:
6513 = Product Number
VVV = Version Number
YWW = Year Week

DFN-12 3x3x0.75 PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Supply voltage	
VDDIO	2	P	Supply voltage for serial bus interface	
SDO	3	DO	4-wire SPI bus: Master input slave output I2C/3-wire SPI bus: Interrupt output	1
SCK	4	DI	I2C & SPI bus: Serial bus clock input	
SDI	5	DI/DO	I2C bus: Serial bus data input / output 4-wire SPI bus: Serial bus data input 3-wire SPI bus: Serial bus data input / output	
CSB	6	DI	Bus type select / chip select with pull-up CSB=VDDIO: I2C mode / chip not selected CSB=GND: SPI mode / chip selected	2
VPP	7	P	Programming voltage for EEPROM write	3
GND	8	G	Power supply ground	
CR	9	AO	Reference capacitance pin	
CC	10	AI	Common capacitance pin	
CS	11	AO	Sensing capacitance pin	
GND	12	G	Power supply ground	
EXP_PAD	-	G	Exposed thermal pad	4

P = Power, G = Ground, DO = Digital Output, DI = Digital Input, AO = Analog Output, AI = Analog Input
Note 1: In I2C and 3-wire SPI protocols the SDO pin must be left unconnected (floating) unless interrupts, external clock or alternative I2C address configuration via SDO pin are used. In 4-wire SPI protocol the SDO pin serves as data output. In Test mode the SDO pin can operate also as test input or output. For further SDO pin configuration details see Configuration register 1 table 8 on page 20. See also application figures 10-11 and 15-16.
Note 2: In I2C mode the unused CSB pin must be left unconnected (floating). The CSB pin has internal 250 kΩ pull-up resistor to VDDIO. To minimize current consumption the pin should be kept high (at VDDIO) except during chip select events of SPI bus communication mode. In Test mode the SDI pin can operate also as test input or output.
Note 3: EEPROM programming voltage is needed only in EEPROM write. In read only applications the VPP pin should be grounded.
Note 4: On PCB the exposed pad is recommended to be connected to GND for minimum noise. It could be also left floating but it cannot be connected to any other potential than GND.

PACKAGE (DFN-12 3X3x0.75) OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.7	0.75	0.8	mm
A1	0	0.035	0.05	mm
b	0.17	0.22	0.27	mm
D	3 BSC			mm
E	3 BSC			mm
e	0.45 BSC			mm
J (Exposed.pad)	1.6	1.7	1.8	mm
K (Exposed.pad)	2.3	2.4	2.5	mm
L	0.35	0.4	0.45	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.

ORDERING INFORMATION

Product Code	Product	Description
MAS6513CA1WA300	Capacitive Sensor Interface IC	Tested inked wafer, thickness 395 µm ± 5%
MAS6513CA1WA313	Capacitive Sensor Interface IC	Tested non-inked wafer with wafer map, thickness 395 µm ± 5%
MAS6513CA1WA305	Capacitive Sensor Interface IC	Bare die in tray, thickness 395 µm ± 5%
MAS6513CA1WAB05	Capacitive Sensor Interface IC	Bare die in tray, thickness 180 µm ± 5%
MAS6513CA1D1008	Capacitive Sensor Interface IC	DFN-12 3x3x0.75, Pb-free, RoHS compliant, loose components (samples only)

Contact Micro Analog Systems Oy for other wafer and die thickness options and volume orders in DFN package.

LOCAL DISTRIBUTOR

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