MAS6287

IC FOR 8.00 – 52.00 MHz VCTCXO

- **Six Curve Compensation**
- **Frequency Stability ± 1 ppm**
- **Wide Range of Frequency**
- **Very Low Phase Noise**
- **Ultra Wide Temperature Range –60 °C … +125 °C**
- **EEPROM Selectable Output**

DESCRIPTION

The MAS6287 is an integrated circuit well suited to build low cost VCTCXO for wide temperature range applications. The trimming data is transferred through a serial bus and the calibration information is stored in an internal EEPROM.

To build a VCTCXO only crystal is required in addition to MAS6287. The compensation method is fully analog, working continuously without generating any steps or other interference.

FEATURES

- Very small size
- Minimal current consumption
- Very low phase noise
- Ultra wide operating temperature range
  - –60 °C … +125 °C
- Output frequency selectable by EEPROM
  - direct f_c or divided $f_c/2$
- Two different pin-out options for module assembly
  - BA1
  - BA2

APPLICATIONS

BLOCK DIAGRAM

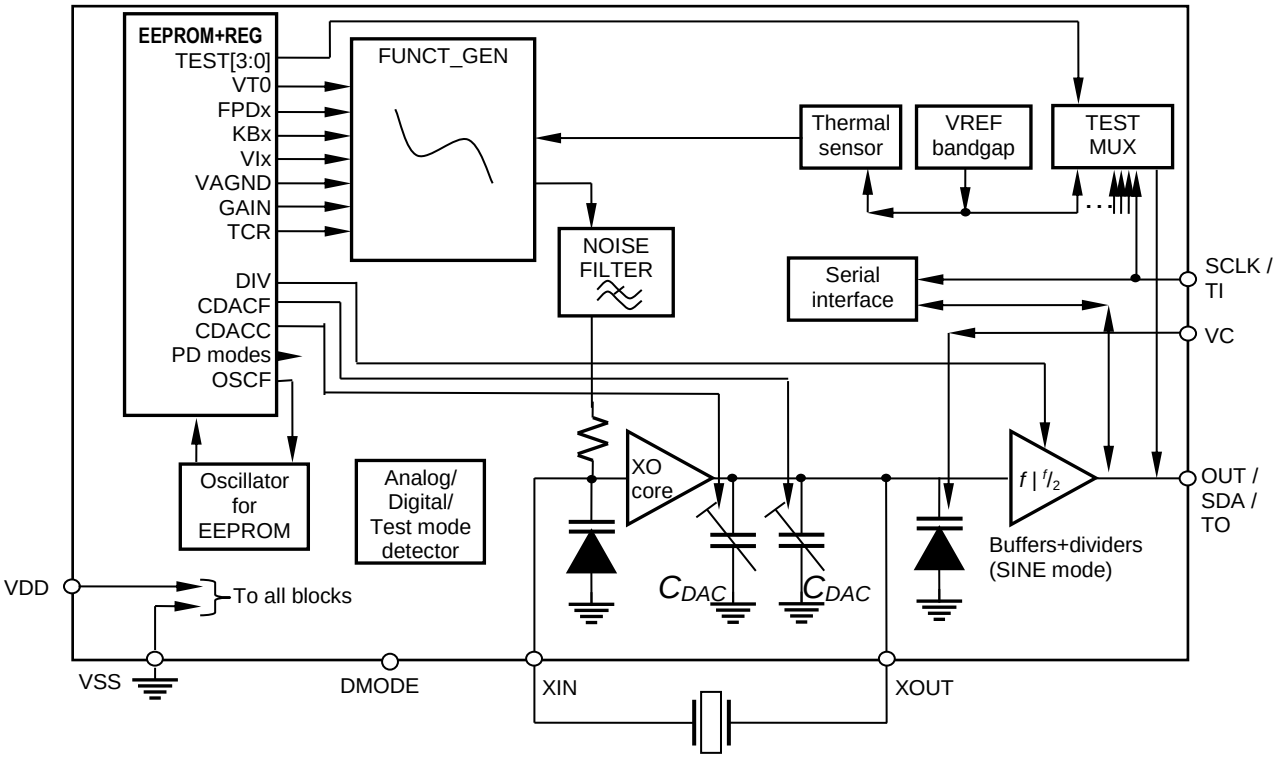


Figure 1. Block diagram of MAS6287

BLOCK DESCRIPTION

MAS6287 block diagram is shown in Figure 1.

VCTCXO consists of external crystal, XO core, trimming CDACs and varactors. By coarse CDAC it is possible to trim frequency at room temperature with large steps and fine CDAC is for additional trimming with smaller steps. One varactor is for tuning with external voltage from VC pin and second varactor is controlled by internal voltage from thermal compensation function generator.

Output buffer includes divide by two function, so output frequency which is half of crystal frequency can be selected by control bit.

On-chip thermal sensor gives temperature info for thermal compensation function generator and bandgap block gives stable reference voltage. XO and function generator are supplied by two voltage regulators.

Trimming coefficients are stored in EEPROM, there is additional oscillator for EEPROM functions.

Serial interface enables to read and write registers and EEPROM. Test mux is for accessing internal signals for test purposes.

Important note: For detailed part description see DAE6287 datasheet extension document which is available upon request from Micro Analog Systems Oy.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	$V_{DD} – V_{SS}$	-0.3	3.6	V	
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} + 0.3	V	
Storage Temperature	T_{ST}	–55	150	°C	
Latchup Current Limit	I_{LUT}	±100		mA	

Note: Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.8	3.3	3.6	V	
Operating Temperature	T_{OP}		–60	25	+125	°C	
Crystal Pulling Sensitivity	S	T_{OP}		40		ppm/pF	
Crystal cut angle		T_{OP}		7		’	1
Crystal Frequency change in temperature (uncompensated)		T_{OP}	-30		45	ppm	
Crystal inflection temperature	T_{inf}		25	29	33	°C	
Crystal frequency offset			-15		15	ppm	
Crystal Load Capacitance	C_L	VC = 1.65V		5.2		pF	
Crystal Rs	Rs			30	60	Ω	
Oscillator Negative Resistance			80			Ω	

Note 1: The crystal cut angle values are in angular minutes (1‘=1/60th of 1°) relative to AT-cut crystal angle 35° 15’.

ELECTRICAL CHARACTERISTICS

(recommended operating conditions)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit	Note
Crystal Frequency Range		f_c		16	26	52	MHz	1)
Output Frequency Range		f_o		8		52	MHz	1)
Voltage Control Range		VC		0	1.65	V_{DD}	V	2)
VC Varactor Nominal Tuning Range			VC_{NOM}+1.65V VC_{NOM}-1.65V		+6.5 -15		ppm	3)
Voltage Control Sensitivity		VC_{SENS}	VC_{NOM}+1V VC_{NOM}-1V		+5.2 -8.9		ppm/V	3)
Voltage Control Linearity		VC_{LIN}			±8.5		%	4)
Frequency vs. Supply Voltage		df_o			±0.06	±0.2	ppm	5)
Frequency vs. Load Change		df_o			±0.03	±0.2	ppm	6)
Output voltage (10 kΩ || 10 pF)		V_{out}	Clipped sine output CBUF=0	0.8	1.9		Vpp	7)
Output voltage (10 kΩ || 10 pF)	High	V_{out}	CMOS output CBUF=1	80%		100%	VDD	
	Low			0%		20%		
DMODE pad pull-down resistor					330		kOhm	
Supply Current, Sine mode		I_{DD}	16 MHz 26 MHz 40 MHz 52 MHz		1.8 2.1 2.5 2.7		mA	
Compensated Frequency Stability		df_o	T_{OP}, S, VC=1.65V	-1		+1	ppm	
CDACC Nominal Tuning Range			S=40ppm/pF	-35		35	ppm	
CDACC Nominal Tuning Step			S=40ppm/pF		1.4		ppm	
CDACF Nominal Tuning Range			S=40ppm/pF	-0.8		0.8	ppm	
CDACF Nominal Tuning Step			S=40ppm/pF		0.11		ppm	
Tcomp Varactor Nominal Tuning Range			S=40ppm/pF	-50		40	ppm	
Amplitude Start up Time		T_{START}			2		ms	8)
Phase Noise	@ 1Hz	φ_n	40MHz, CMOS output		-47		dBc/Hz	8)
	@ 10Hz				-80			
	@ 100Hz				-111			
	@ 1kHz				-134			
	@ 10kHz				-145			
	@ 100kHz				-149			

Note 1: Frequency division by two is selected by EEPROM bit DIV: 0=no division, 1=div by 2
Thus, IC output frequency range is 8 MHz – 52 MHz.
Note 2: If VC is not needed, corresponding EEPROM bit should be selected and VC pin to be left floating.
Note 3: Depending on a crystal pulling. Different at different VC voltages.
Note 4: Best fit line. VC=1.65V ± 1.0V, V_{DD}=3.3V
Note 5: V_{DD} ± 5%
Note 6: R_L = 10 kΩ ± 10% C_L = 10 pF, R_L = 10 kΩ C_L = 10 pF ± 10%
Note 7: Sine mode only, clipped sine output.
Note 8: 40MHz crystal. Not measured in production testing.
Note 9: Max load at OUT pin 5kΩ, 40pF

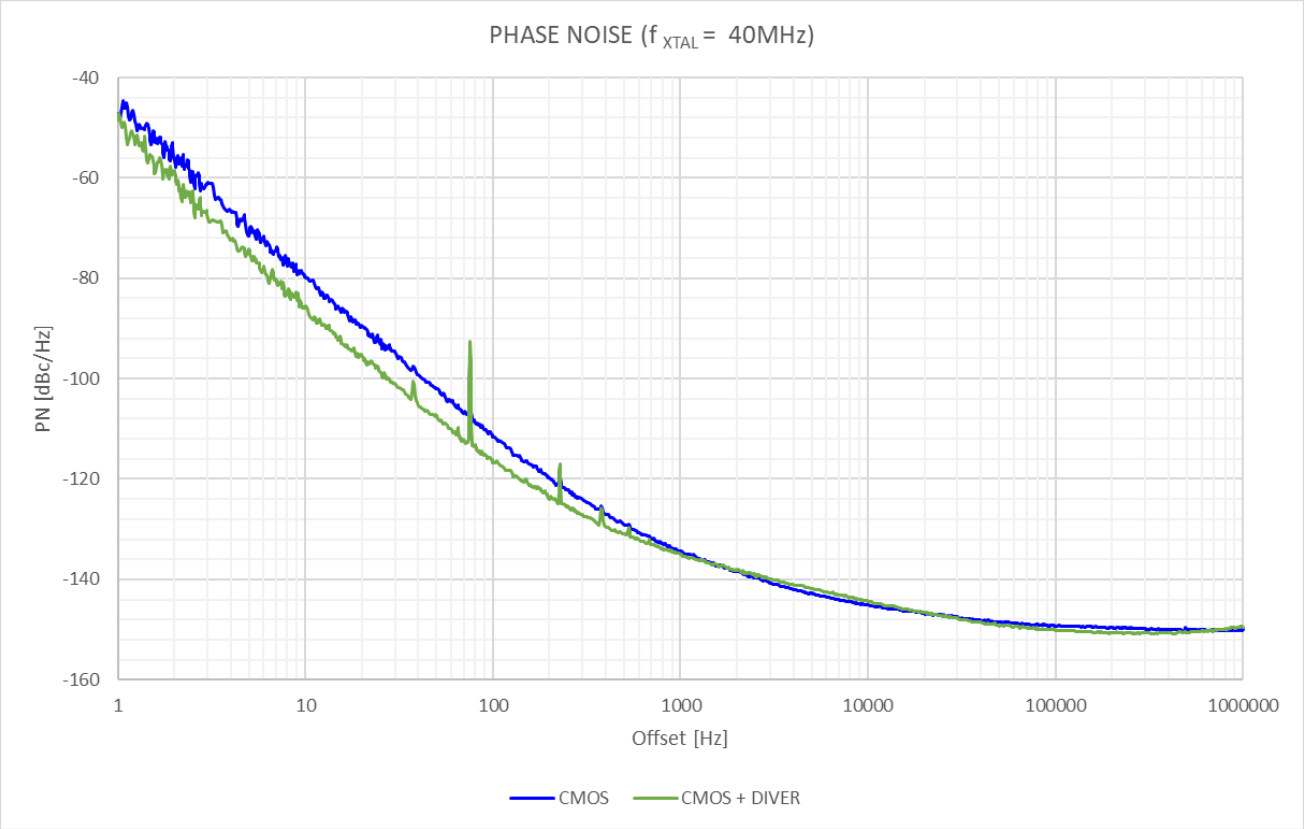


Figure 2. MAS6287BA phase noise with 40MHz crystal and CMOS output

OPTIMAL CRYSTAL CHARACTERISTICS

For temperature range –60°C…+125°C the optimal AT-cut crystal's temperature characteristic is like the green colored 7' cut angle curve shown in the figure 3 below. The crystal variations should be kept within MIN and MAX curves with cut angle ranging from 6' to 8'. Additionally, high crystal pulling (typ 40 ppm/pF) is needed for the successful temperature compensation.

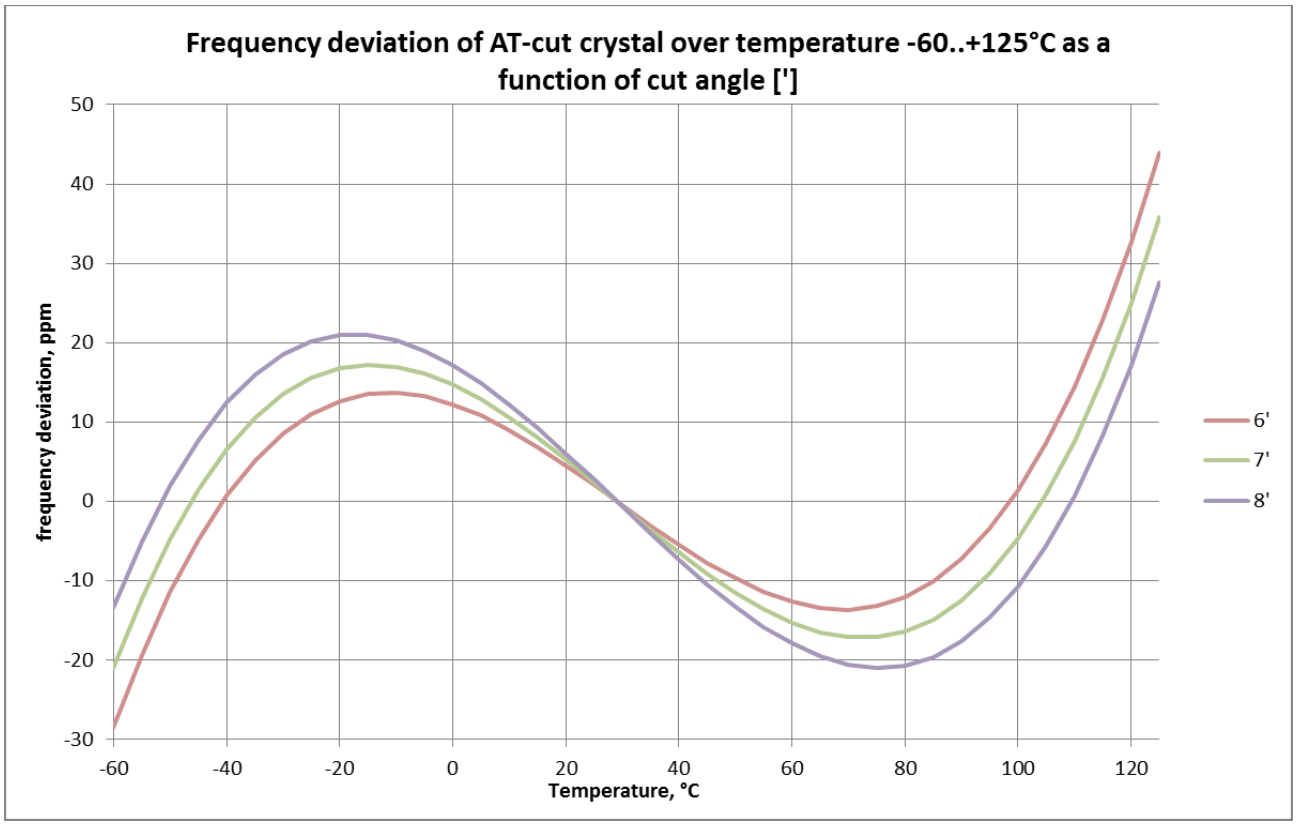


Figure 3. Range of temperature characteristics of suitable AT-cut crystals (curves plot having 0ppm reference set to +28°C)

For higher temperature ranges, the optimum crystal parameters change. Generally, the wider the range for temperature compensation, the higher the crystal cutting angle. It can be explained by the high roll-off of crystal thermal characteristics at extreme temperatures, which are optimized by allowing higher deviation at the lower and higher turnover points so that the deviation at extreme temperatures becomes smaller, when compared to crystals having smaller cutting angles.

DEVICE OUTLINE CONFIGURATION

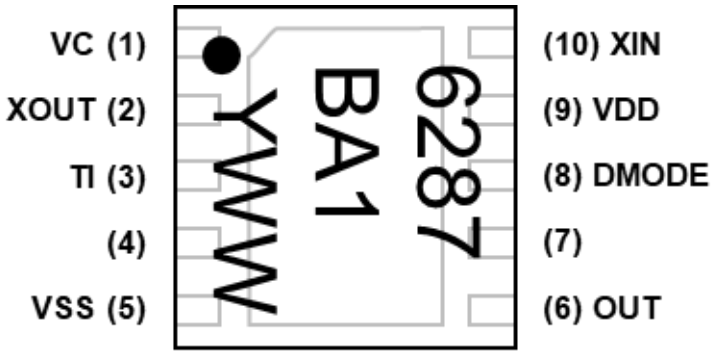


Figure 4. MAS6287BA1 in DFN-10 3x3x0.75mm package

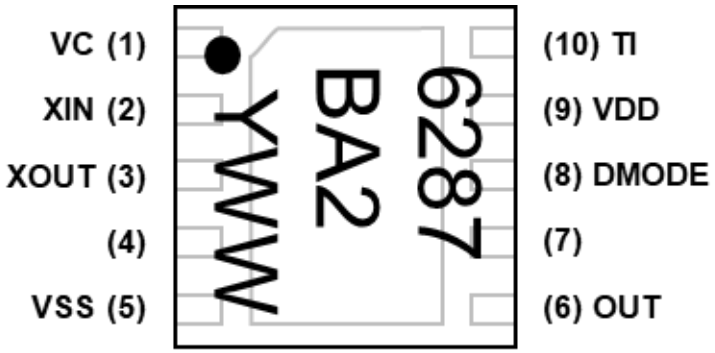


Figure 5. MAS6287BA2 in DFN-10 3x3x0.75mm package

DFN-10 3x3x0.75 PIN DESCRIPTION

Pin Number	BA1 Pin Name	BA2 Pin Name	Function	Notes
1	VC	VC	Voltage Control Input	
2	XOUT	XIN	BA1: Crystal Output. BA2: Crystal Input.	
3	TI	XOUT	BA1: Test Input. BA2: Crystal Output.	1
4				2
5	VSS	VSS	Supply Ground	
6	OUT	OUT	RF Output	1
7				2
8	DMODE	DMODE	Digital Mode Control Input	1
9	VDD	VDD	Supply Voltage	
10	XIN	TI	BA1: Crystal Input. BA2: Test Input.	
EXP_PAD			Expose Thermal Pad	2

Note 1: In analog mode (DMODE=low) TI pin operates as Test Input and OUT pin as RF Output or Test Output (TO). In digital mode (DMODE=high) TI pin operates as serial bus clock input (SCLK) and OUT pin as bi-directional serial data input/output (SDA).
Note 2: On PCB the unconnected pins 4 and 7 and exposed thermal pad are recommended to be connected to GND.

DEVICE OUTLINE CONFIGURATION

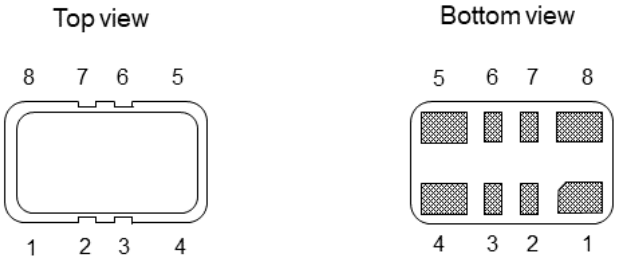


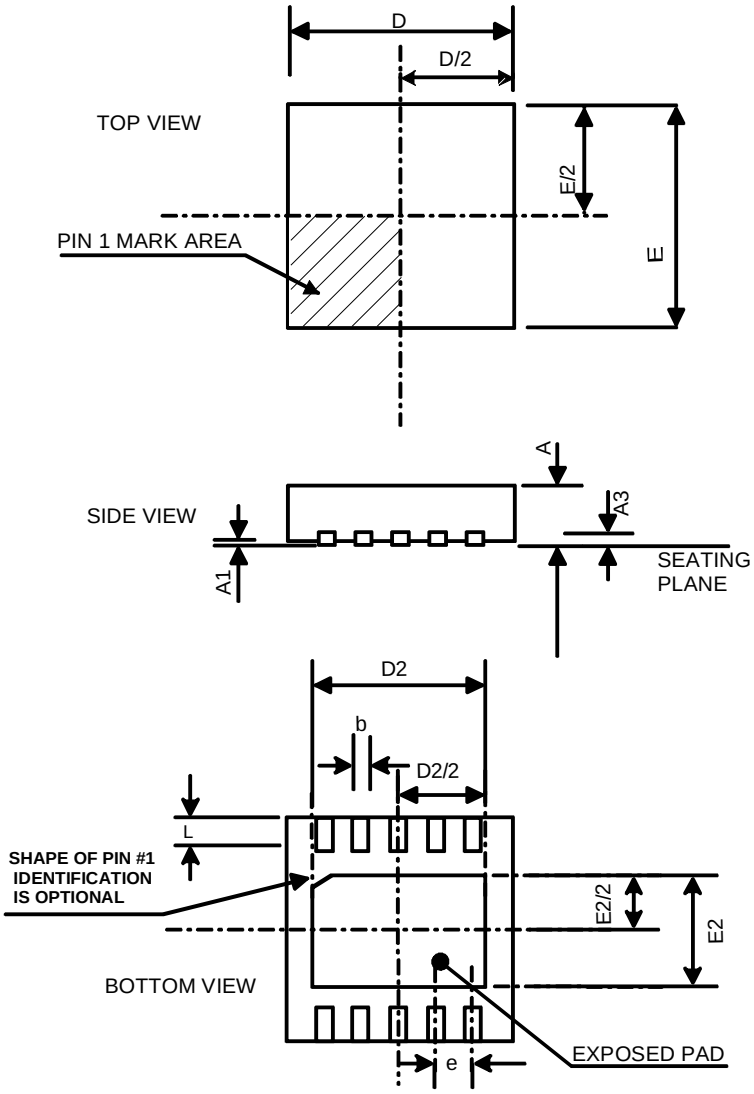
Figure 6. Device outline of 5032 size MAS6287BA2 module

5032 MODULE PIN DESCRIPTION

Pin Number	BA2 Pin Name	Function	Notes
1	VC	Voltage Control Input	
2			1
3	TI	Test Input	2
4	VSS	Supply Ground	1
5	OUT	RF Output	2
6	DMODE	Digital Mode Control Input	2
7-8	VDD	Supply Voltage	3

Note 1: On PCB the unconnected pin 2 is recommended to be connected to GND.
Note 2: In analog mode (DMODE=low) TI pin operates as Test Input and OUT pin as RF Output or Test Output (TO). In digital mode (DMODE=high) TI pin operates as serial bus clock input (SCLK) and OUT pin as bi-directional serial data input/output pin (SDA).
Note 3: VDD pins 7 and 8 are connected together inside module

PACKAGE (DFN-10 3x3x0.75) OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3	0.178	---	0.228	mm
b	0.200	---	0.300	mm
D	2.950	3.000	3.050	mm
D2 (Exposed.pad)	2.500	---	2.700	mm
E	2.950	3.000	3.050	mm
E2 (Exposed.pad)	1.650	---	1.750	mm
e		0.500 BSC		mm
L	0.350	---	0.450	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.

ORDERING INFORMATION

Product Code	Product	IC Outline	Package
MAS6287BA1WA900	IC for VCTCXO	BA1	EWS Tested wafer 215 µm
MAS6287BA1WA905	IC for VCTCXO	BA1	Tested bare die in tray, thickness 215 µm
MAS6287BA2WA900	IC for VCTCXO	BA2	EWS Tested wafer 215 µm
MAS6287BA2WA905	IC for VCTCXO	BA2	Tested bare die in tray, thickness 215 µm

Contact Micro Analog Systems Oy for other wafer thickness options.

LOCAL DISTRIBUTOR

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