# MAS6230

## High Efficiency 60W Synchronous Buck-Boost DC/DC Converter

- **Wide Input Voltage Range from 7V to 36V**
- **Adjustable Output Voltage from 4V to 20V**
- **Up to 60W Output Power**
- **Very High Efficiency >90%**
- **Up to 3A Output Current (Buck Mode)**
- **Over Temperature Protection**
- **Output Overvoltage Protection**
- **Low Quiescent Current**
- **QFN-48 7x7x0.75 mm Package**

## DESCRIPTION

MAS6230 is a power supply solution for cell phone, tablet and laptop cigarette lighter chargers in cars and other vehicles. It comprises of a very high efficiency synchronous buck-boost DC/DC converter which can deliver up to 60W output power. It has both wide 7V to 36V input and 4V to 20V output voltage range covering wide variety of applications. The DC/DC converter has hysteresis between buck and boost modes which makes it stable with wide range of external components.

MAS6230 integrates over temperature (OTP) and output overvoltage protection (OVP) circuitry to prevent damage under fault conditions. The output voltage is adjustable by external feedback resistors. Additionally the output voltage can be selected from four different options using feedback voltage selection pins (FBSEL0-1). This is a useful feature in applications where several different output voltage selections are supported.

The device is available in a thin 7x7x0.75 mm 48-lead QFN package.

## FEATURES

- Wide input voltage range from 7V to 36V
- Output voltage adjustable by 2 external resistors from 4V to 20V
- Four output voltage options selectable by two input pins
- Up to 60W output power
- Over 90% efficiency
- Up to 3A output current (buck mode)
- Low inductance value inductor
- Automatic transition between buck and boost modes
- Over temperature protection
- Output overvoltage protection
- Low quiescent current
- Thin 7x7x0.75 mm QFN-48 package

## APPLICATIONS

- USB-C PD car charger
- Power supply solution for industrial equipment
- Power supply solution for home appliances

## ABSOLUTE MAXIMUM RATINGS

All voltages with respect to ground.

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Pin Voltage | VIN | | -0.3 | 42 | V |
| Output Pin Voltage | VOUT | | -0.3 | 25 | V |
| Internal Power Supply Pin Voltage | VDD | | -0.3 | 6 | V |
| Input Pin Voltage | EN | | -0.3 | VIN+0.3 | V |
| | MEMO, FBSEL0-1, FB, FORCEBUCK | | -0.3 | 6 | V |
| Inductor Switch Pin Voltage | SW1 | | -0.3 | 42 | V |
| | SW2 | | -0.3 | 25 | V |
| Flying Capacitor Pin Voltage | FLY1A/B, FLY2A/B | | -0.3 | 42 | V |
| Storage Temperature | $T_{STG}$ | | -40 | +125 | ºC |
| ESD Voltage Rating | $V_{HBM}$ | Human Body Model (HBM) | ±1 | | kV |
| | $V_{CDM}$ | Charged-Device Model (CDM) | ±500 | | V |

**Note:** Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.
**Note:** JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
**Note:** JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## RECOMMENDED OPERATING CONDITIONS

All voltages with respect to ground.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Junction Temperature | $T_J$ | | -40 | | +125 | °C |
| Operating Ambient Temperature | $T_A$ | | -40 | +27 | +85 | °C |
| Operating Supply Voltage | $V_{IN}$ | | 7.0 | | 36.0 | V |
| Operating Output Voltage | $V_{OUT}$ | | 5 | | 20 | V |
| Output Current | $I_{OUT}$ | Buck mode ($V_{IN} \geq V_{OUT}$) Note 1 | | | 3.0 | A |
| Inductor Specification | L | Shielded inductor Note 2 | 4 | 6.8 | 13 | µH |
| | $I_{RATED}$ | | | 6 | | A |
| | $R_{DC}$ | | | 27 | | mΩ |

**Note 1:** In boost mode the maximum output current may be lower due to coil current limiting. For further information see figure 4 on page 7.
**Note 2:** See inductor examples in table 1 on page 6.

## ELECTRICAL CHARACTERISTICS

$T_A$ = -40°C to +85°C, typical values at $T_A$ = 27°C, $V_{IN}$ = 20 V, L=6.8 µH; unless otherwise specified

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{IN}$ | | 7 | | 36 | V |
| Output voltage range | $V_{OUT}$ | | 4 | | 20.5 | V |
| Internal supply voltage(1) | $V_{DD}$ | VIN=20V | 3.0 | 4.5 | 5.5 | V |
| Efficiency | η | $I_{OUT}$=3A, $V_{IN}$=30V, $V_{OUT}$=20V<br>(buck mode) | | 92.4 | | % |
| Feedback voltage | $V_{FB}$ | $V_{IN}$=20V<br>FBSEL1/0=LOW/LOW<br>FBSEL1/0=LOW/HIGH<br>FBSEL1/0=HIGH/LOW<br>FBSEL1/0=HIGH/HIGH | <br>1170<br>877<br>526<br>291 | <br>1200<br>900<br>540<br>300 | <br>1230<br>923<br>554<br>315 | <br>mV |
| Valley coil current limit | $I_{COIL\_LIM}$ | L=6.8 µH | 3.3 | 3.8 | 4.3 | A |
| Peak coil current limit | $I_{COIL\_PEAK}$ | L=6.8 µH | | 5.3 | 6.3 | A |
| On resistances of High side switches | $R_{HON1}$<br>$R_{HON2}$ | | | 30<br>50 | | mΩ |
| On resistances of Low side switches | $R_{LON1}$<br>$R_{LON2}$ | | | 50<br>50 | | mΩ |
| Shutdown current | $I_{SD}$ | EN=LOW, VOUT=0V | | TBD | | µA |
| Undervoltage lockout threshold voltage | $V_{UVLO+}$<br>$V_{UVLO-}$ | $V_{IN}$ rising<br>$V_{IN}$ falling | 6.2<br>5.85 | 6.6<br>6.3 | 7<br>6.65 | V |
| Undervoltage lockout hysteresis | $V_{UVLOH}$ | $V_{IN}$ rising | | 300 | | mV |
| Input high voltage | $V_{IH}$ | Pins EN, FBSEL0-1,<br>FORCEBUCK | 1.2 | | | V |
| Input low voltage | $V_{IL}$ | Pins EN, FBSEL0-1,<br>FORCEBUCK | | | 0.4 | V |
| Input current | IIH | Pins EN, FBSEL0-1,<br>FORCEBUCK<br>Input voltage = 3.5V, VIN = 20V | | <br><br>0.01 | <br><br>1 | <br><br>µA |
| | IIL (2) | Pins EN, FBSEL0-1,<br>FORCEBUCK, VIN = 20V<br>Input voltage = 0V<br>Input voltage = 0.4V | | <br><br>0.01<br>1 | <br><br>1<br>2 | <br><br>µA |
| Output overvoltage protection | | | 21 | 23.5 | 25 | V |
| Over temperature protection | | | 135 | 150 | 165 | ºC |
| Over temperature hysteresis | | | | 10 | | ºC |

**Note 1:** Internal supply voltage at VDD pin is only for internal circuit use. It should not be loaded externally.
**Note 2:** Digital inputs have active pull-down by 410kΩ which is disabled to save current when inputs are pulled high.
TBD = To Be Defined

## THERMAL INFORMATION

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Junction to ambient thermal resistance | $R_{\theta JA}$ | Note 1 | | 26.6 | | °C/W |

**Note 1:** Simulated value for Jedec JESD51-5 4-layer 1.6mm thick board with 4x4=16 pcs thermal vias under QFN package thermal pad.

## APPLICATION DIAGRAMS

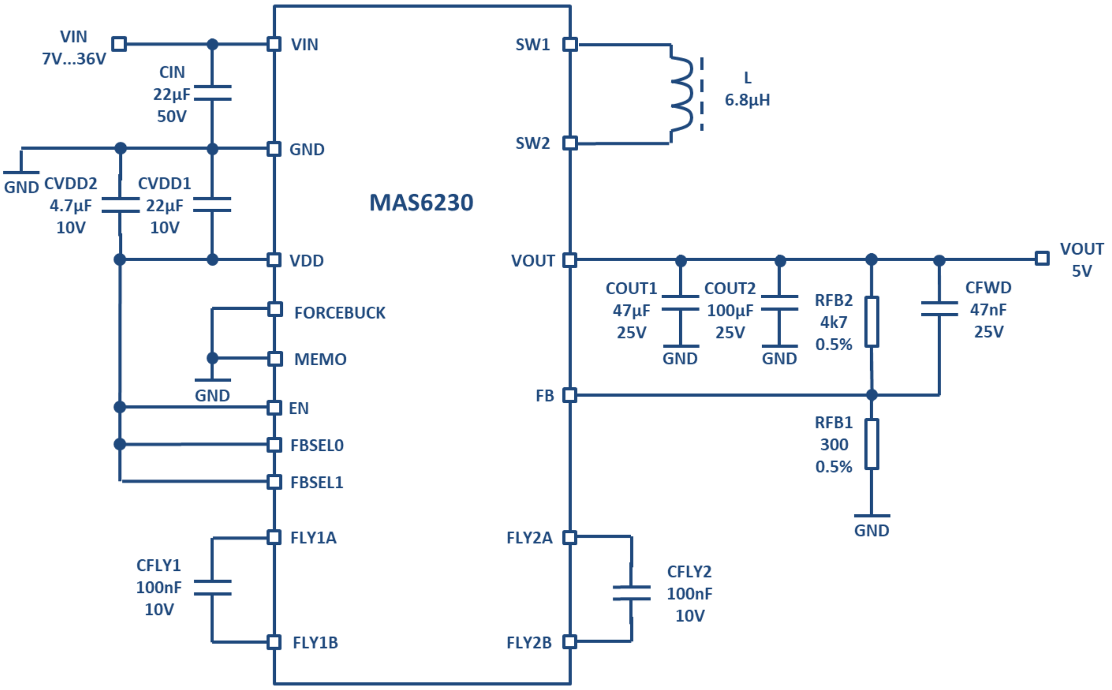



**Figure 1.** MAS6230 application diagram with fixed 5V output

The MAS6230 can be kept enabled always by connecting the EN pin to the VDD pin since the internal supply voltage is available from the VDD pin also in shut down mode.

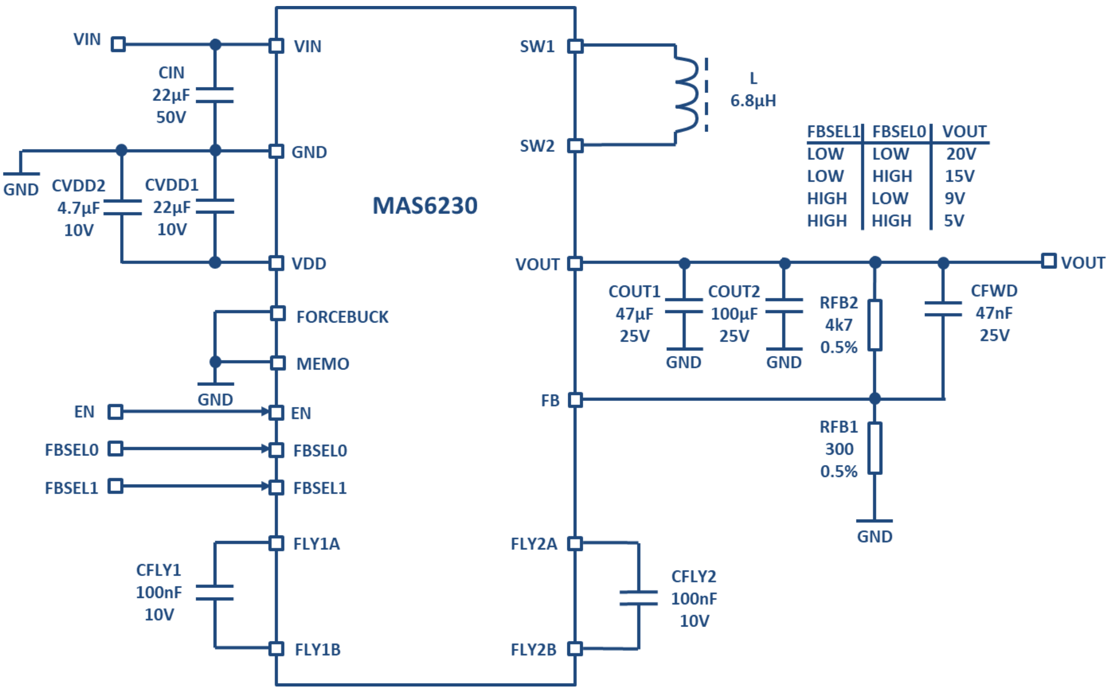



**Figure 2.** General MAS6230 application diagram with four output voltage options using FBSEL0-1 control.

Using FBSEL0-1 control it is possible implement four different selectable output voltages.

## APPLICATION DIAGRAMS (continued)

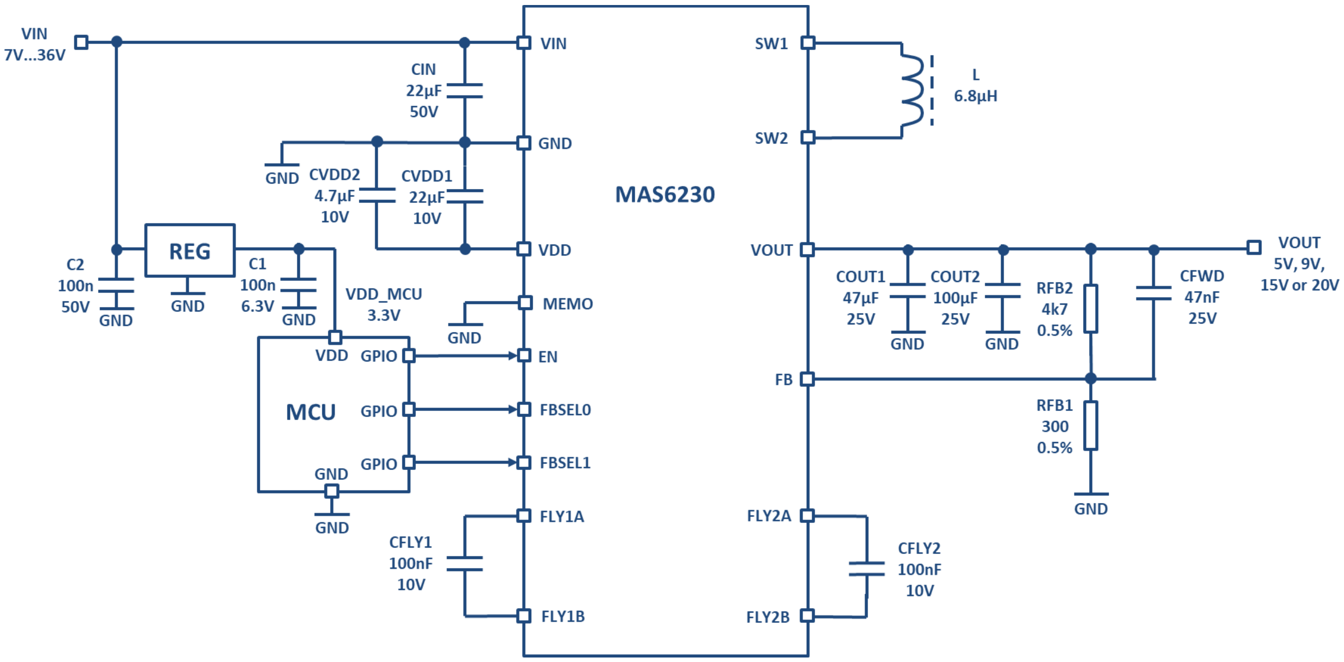



**Figure 3.** MAS6230 application diagram with regulated MCU selecting between four output voltage options

# DETAILED DESCRIPTION

MAS6230 is a high efficiency synchronous buck-boost DC/DC converter with both wide input and output voltage range. Four integrated low resistance N-channel power transistors minimize application solution size and maximize efficiency.

The device is controlled on and off using single enable pin (EN). In shut-down (EN=LOW) the DC/DC converter is turned off and only a small quiescent current is drawn from the input ($V_{IN}$).

When enabled (EN=HIGH) the DC/DC converter is on and selection between buck ($V_{OUT} < V_{IN}$) and boost ($V_{OUT} > V_{IN}$) operating modes is done automatically. There is hysteresis between buck and boost operating modes which makes the DC/DC converter stable with wide range of external components.

The undervoltage lockout (UVLO) circuit prevents the DC/DC converter to operate at too low input voltage conditions. The device enters shut-down if input voltage drops below typ 6.3V independent of enable pin state. When enabled the device is on if input voltage has risen above typ 6.6V.

MAS6230 regulates output voltage ($V_{OUT}$) to level which is adjusted by feedback voltage (VFB) and two feedback resistor values (RFB1, RFB2). See application figures 1-3. The feedback voltage can be selected from four options using FBSEL0-1 pins. This makes it possible to output four different output voltages which are selectable just by FBSEL0-1 pin control as shown in the figures 2-3. See also Output voltage adjustment in the Application information section.

# APPLICATION INFORMATION

## Inductor selection

Inductor needs to be rated typically to 6A or higher current. The dc-resistance of inductor has contribution to power losses and to achieve high efficiency and output power the dc-resistance should be minimized. Table 1 shows two examples of inductors. The larger toroid coil with low dc-resistance is recommended for highest efficiency and highest output power applications. The smaller SMD inductor can be used in more space-constrained applications with lower output power requirement.

**Table 1.** Inductor examples

| Part number | Manuf. | Package | L [μH] | $R_{DC}$ [mΩ] | $I_{RATED}$ [A] |
|---|---|---|---|---|---|
| DTMSS-12.5 | Feryster | Toroid core Ø 12.5mm | 6.8 | 7.22 | 8 |
| XAL5050-682ME | Coilfraft | SMD 5x5x5.1mm | 6.8 | 26.75 | 6 |

## Capacitor selection

All capacitors must be low loss (low ESR) ceramic capacitors. Recommended capacitors values are shown in the table 2. The CFWD=47nF capacitor value is suited to be used with feedback resistor values RFB1=300Ω and RFB2=4.7kΩ.

**Table 2.** Recommended capacitor values

| Capacitor | Nominal value | Voltage rating | Type |
|---|---|---|---|
| CIN | 22μF | 50V | Ceramic MLCC capacitor |
| COUT1 | 47μF | 25V | Ceramic MLCC capacitor |
| COUT2 | 100μF | 25V | Organic polymer capacitor |
| CVDD1 | 22μF | 10V | Ceramic MLCC capacitor |
| CVDD2 | 4.7μF | 10V | Ceramic MLCC capacitor |
| CFLY1 | 100nF | 10V | Ceramic MLCC capacitor |
| CFLY2 | 100nF | 10V | Ceramic MLCC capacitor |
| CFWD | 47nF | 25V | Ceramic MLCC capacitor |

## APPLICATION INFORMATION (continued)

### Output voltage adjustment

MAS6230 produces regulated output voltage (VOUT) which depends on selected feedback voltage option (VFB) and feedback resistor values (RFB1, RFB2) as described in the equation 1. See also figures 1 and 2 for the feedback resistor configuration.

$$VOUT = VFB \cdot \left(1 + \frac{RFB2}{RFB1}\right)$$ **Equation 1.**

There are four different feedback voltage (VFB) options selectable by the FBSEL0-1 pins. See table 3.

**Table 3.** Feedback voltage selection options

| FBSEL1 | FBSEL0 | VFB [V] |
|---|---|---|
| GND | GND | 1.2 |
| GND | VDD | 0.9 |
| VDD | GND | 0.54 |
| VDD | VDD | 0.3 |

For example by choosing RFB2=4.7kΩ and RFB1=300Ω the four standard output voltages 20V, 15V, 9V and 5V are selectable using the FBSEL0-1 pins.

FBSEL1/0=GND/GND: $V_{OUT}$=1.2*(1+4.7kΩ / 300Ω) = 20V
FBSEL1/0=GND/VDD: $V_{OUT}$=0.9*(1+4.7kΩ / 300Ω) = 15V
FBSEL1/0=VDD/GND: $V_{OUT}$=0.54*(1+4.7kΩ / 300Ω) = 9V
FBSEL1/0=VDD/VDD: $V_{OUT}$=0.3*(1+4.7kΩ / 300Ω) = 5V

### Maximum output current (typical)

Maximum output current is limited mainly by heating effect. The power losses should be kept below max 2.5W to keep operating junction temperature below max +125°C when ambient temperature is at max +60C°. Second output current limitation comes from coil current limiting of MAS6230. This output current limitation can take place in boost operating mode ($V_{IN}$ < $V_{OUT}$) at which input current is increased. Figure 4 illustrates maximum output currents (IOUT[A] max) in typical case at different input voltages (VIN[V]) and at four output voltage options 5V, 9V, 15V and 20V.

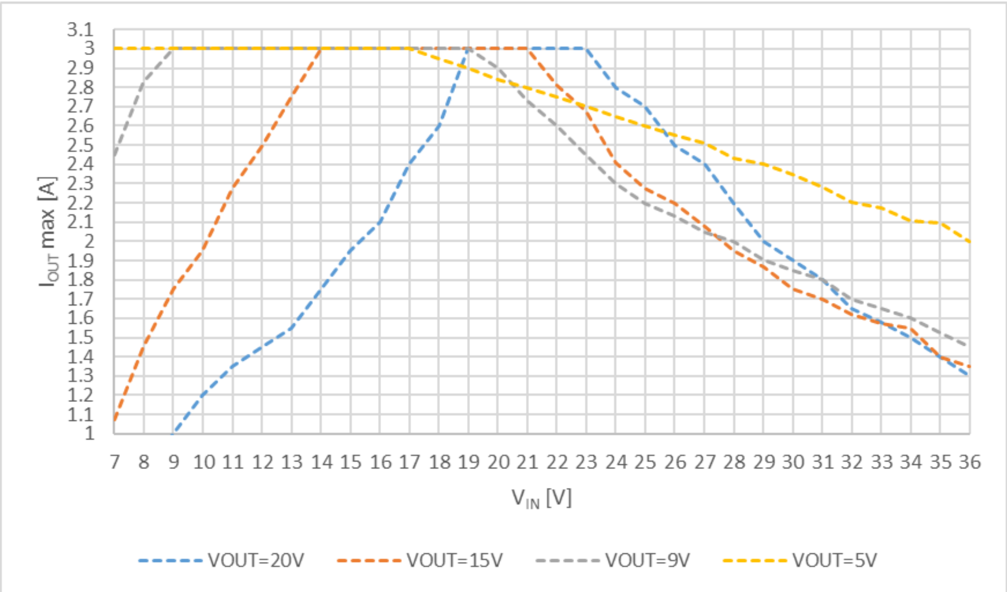



**Figure 4.** Typical MAS6230 maximum output currents ($I_{OUT}$ max) at different input ($V_{IN}$) and output ($V_{OUT}$) voltages

## THERMAL DESIGN CONSIDERATIONS

MAS6230 is a high power device which can output up to 60W power to load. It has high efficiency but at maximum output loading the power losses can be over two watts. This puts special attention to printed circuit board (PCB) thermal design to avoid device overheating.

Heat transfer capability from silicon die to ambient is described by thermal resistance ($R_{\theta JA}$) which is ratio of temperature difference ($\Delta T_{JA}$) between silicon junction and ambient and power loss ($P_{loss}$). See equation 2.

$$R_{\theta JA[°C/W]} = \frac{\Delta T}{P_{loss}} = \frac{T_J - T_A}{P_{loss}}$$ **Equation 2.**

Thermal resistance must be low enough to keep the silicon junction temperature below maximum specified operating junction temperature at maximum ambient temperature and power loss conditions. Using equation 2 we can calculate maximum thermal resistance for conditions $T_J$(max)=+125°C, $T_A$(max)=+60°C and $P_{loss}$(max)=2.5W.

$$R_{\theta JAmax[°C/W]} = \frac{125°C - 60°C}{2.5W} = 26°C/W$$

Thermal resistance is characteristic of package and thermal design of the PCB. The QFN package contains exposed thermal pad which offers an effective heat transfer path from the silicon die to the PCB. On PCB the thermal heat transfer can be considered taking place only via metal layers since copper has 400-1400 times larger thermal conductivity than the insulating FR-4 substrate. To achieve sufficiently low thermal resistance it is necessary to use thermal vias under the exposed thermal pad and to connect the vias to inner and other available layer continuous metal planes on a multi-layer board. In thermal design the key point is to transfer the heat from component to continuous metal planes which spread the heat to wider PCB area wherefrom it can further transfer to ambient.

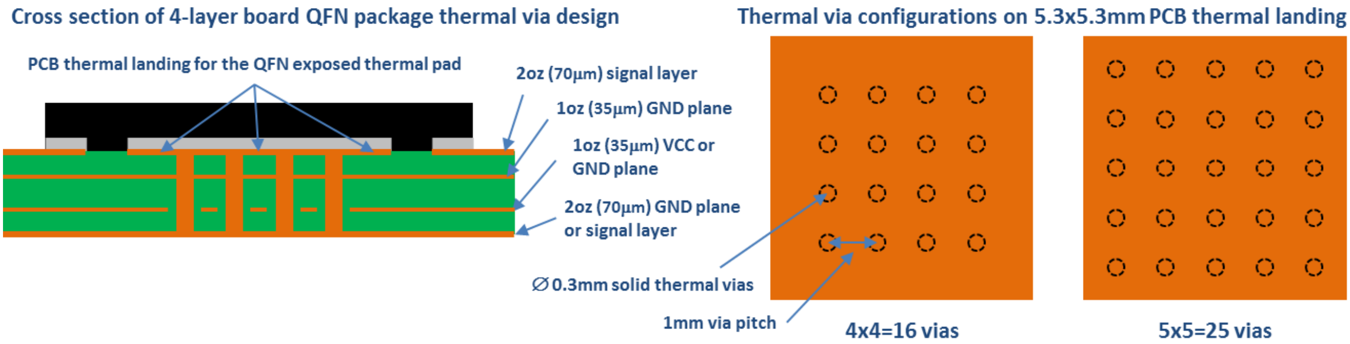



**Figure 5.** QFN 7x7 package thermal via design illustration on a 4-layer board

Figure 5 illustrates QFN 7x7 package thermal via design on a multi-layer board. Board and via parameters are listed in table 3.

**Table 3.** Low thermal resistance PCB design parameters for the QFN-48 7x7mm package

| Parameter | Unit | Value | Note |
|---|---|---|---|
| Finished PCB thickness | mm | 1.6 | |
| Layers | pcs | 4 | |
| Copper thicknesses<br>Top/Bottom<br>Inner layers | oz (µm) | 2 (70)<br>1 (35) | As many as possible continuous GND planes connected to QFN package exposed thermal pad using thermal vias |
| PCB thermal landing | mm | 5.3x5.3 | Same as QFN package exposed pad size |
| Thermal via<br>Diameter<br>Pitch | mm | 0.3<br>1 | Solid thermal vias |
| Thermal via configuration | pcs | 4x4=16 or 5x5=25 | |

MICRO ANALOG SYSTEMS

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

**Output voltage stability (typical)**

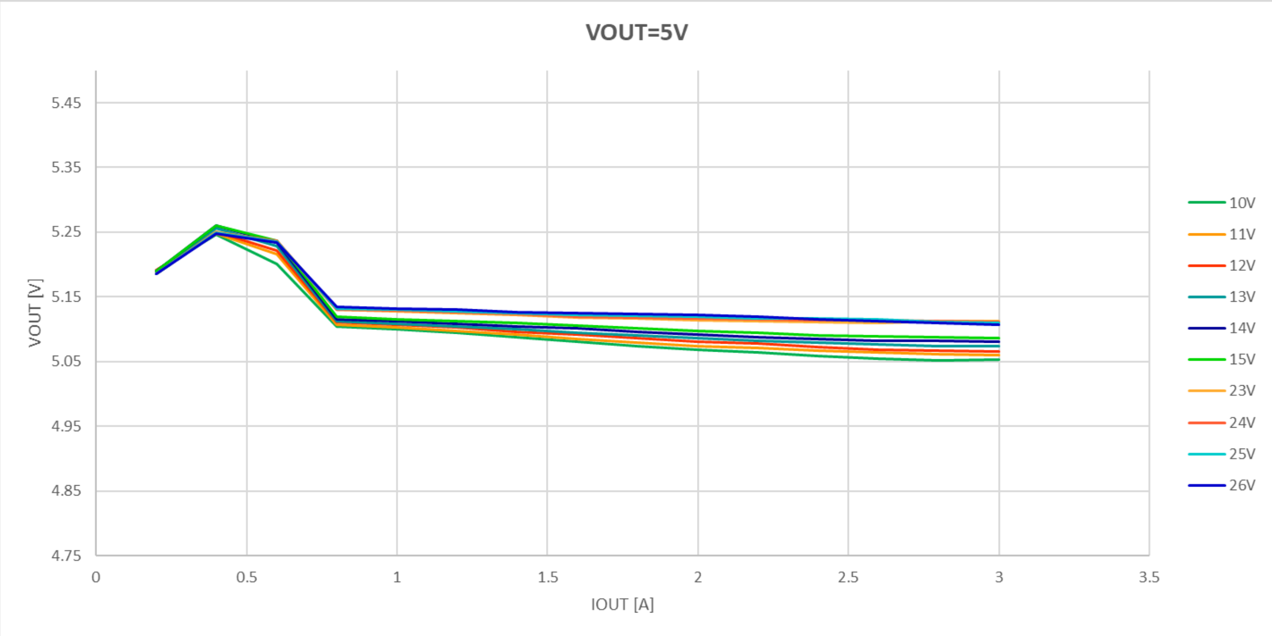



**Figure 6.** Output voltage VOUT[V] vs. output current IOUT[A] at VOUT=5V selection and at different VIN[V]

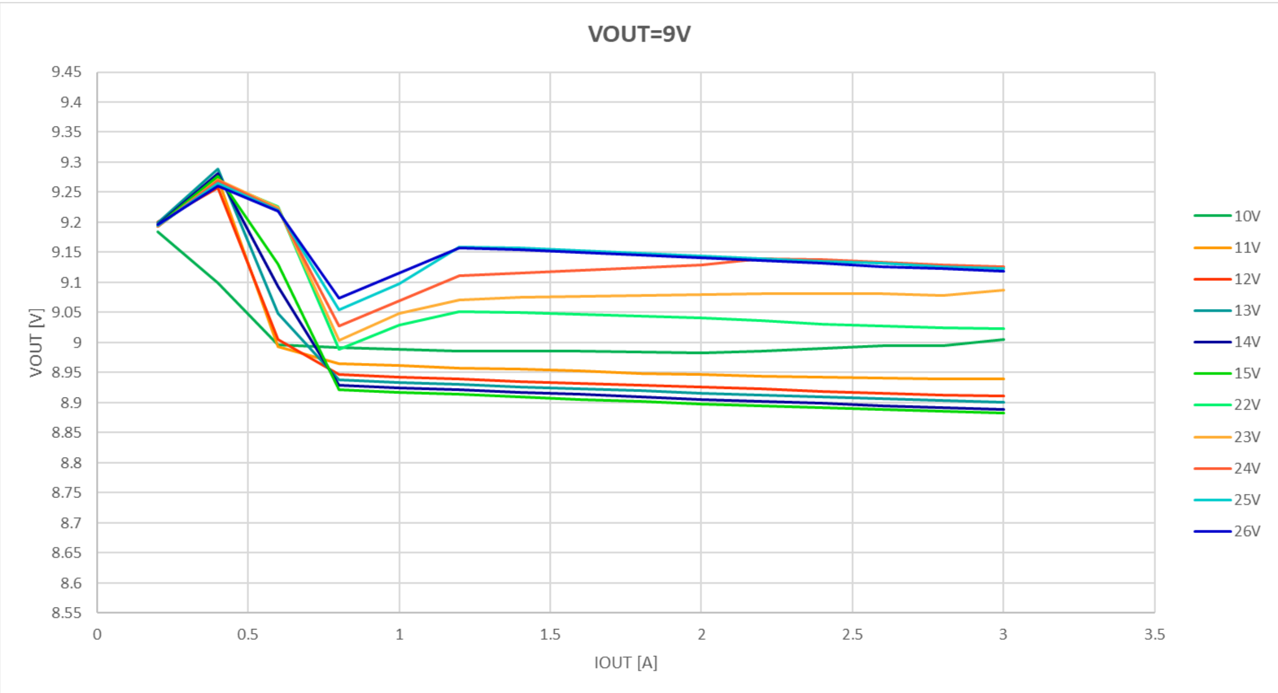



**Figure 7.** Output voltage VOUT[V] vs. output current IOUT[A] at VOUT=9V selection and at different VIN[V]

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (continued)

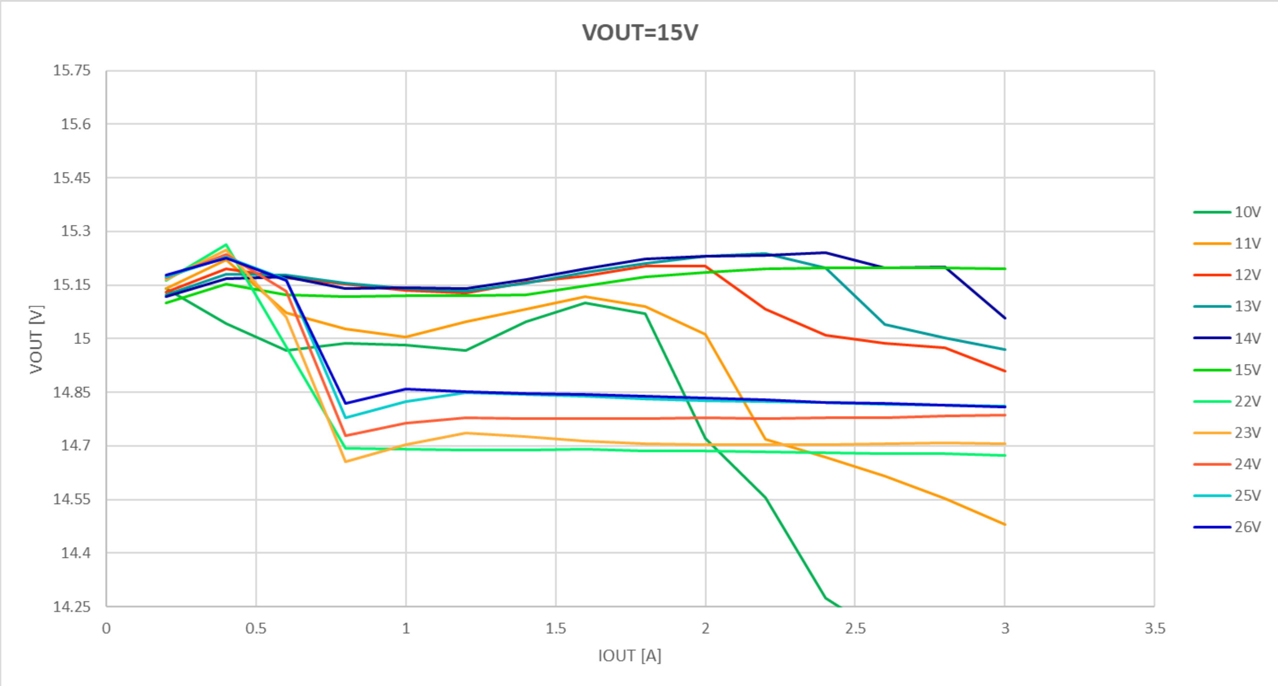



**Figure 8.** Output voltage VOUT[V] vs. output current IOUT[A] at VOUT=15V selection and at different VIN[V]

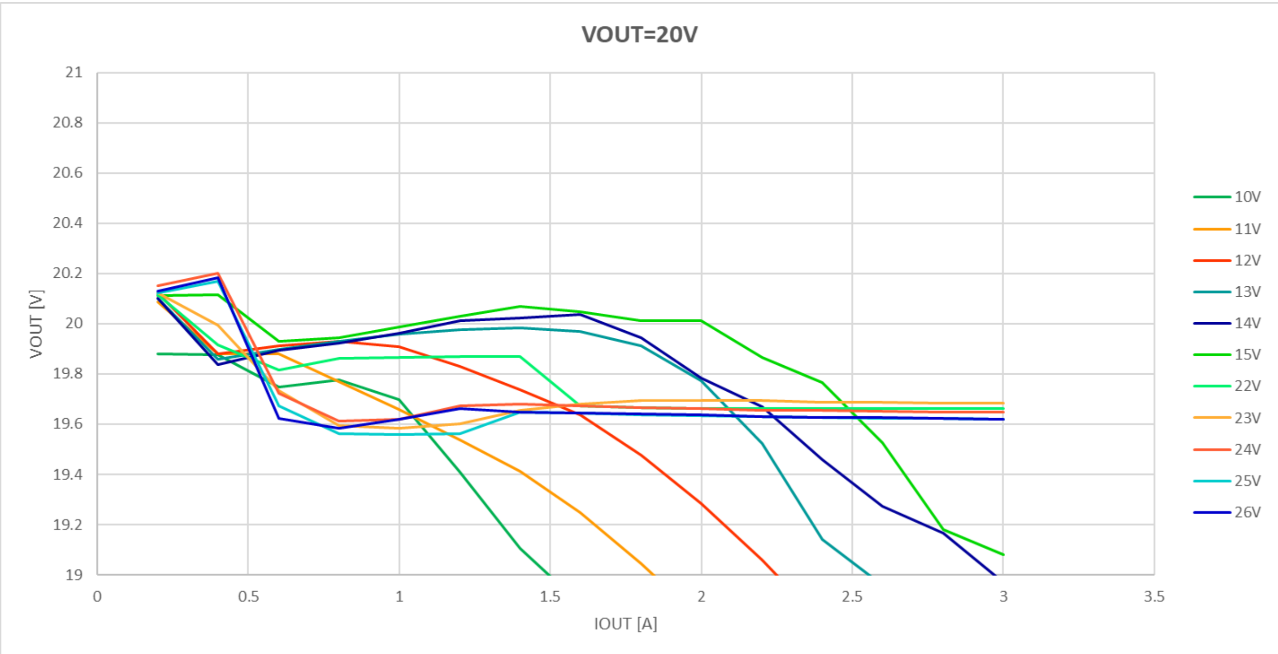



**Figure 9.** Output voltage VOUT[V] vs. output current IOUT[A] at VOUT=20V selection and at different VIN[V]

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (continued)

**Efficiency (typical)**

The efficiency figures 10-13 include also two calculated efficiency curves (dashed lines) corresponding to 2W and 2.5W power losses. Required minimum efficiency (η min) for maximum power loss (Ploss max) can be calculated from equation 3.

$$\eta_{min}[\%] = 100\% \cdot \frac{P_{out}}{P_{loss\,max}+P_{out}} = \frac{100\%}{\frac{P_{loss\,max}}{P_{out}}+1} = \frac{100\%}{\frac{P_{loss\,max}}{V_{out} \cdot I_{out}}+1}$$ **Equation 3.**

For example if maximum allowed power loss is Ploss max =2.5W the minimum required efficiency at VOUT=5V, IOUT=3A (POUT=15W) would be η min =100%/[2.5W/(5V*3A)+1]=85.7%.

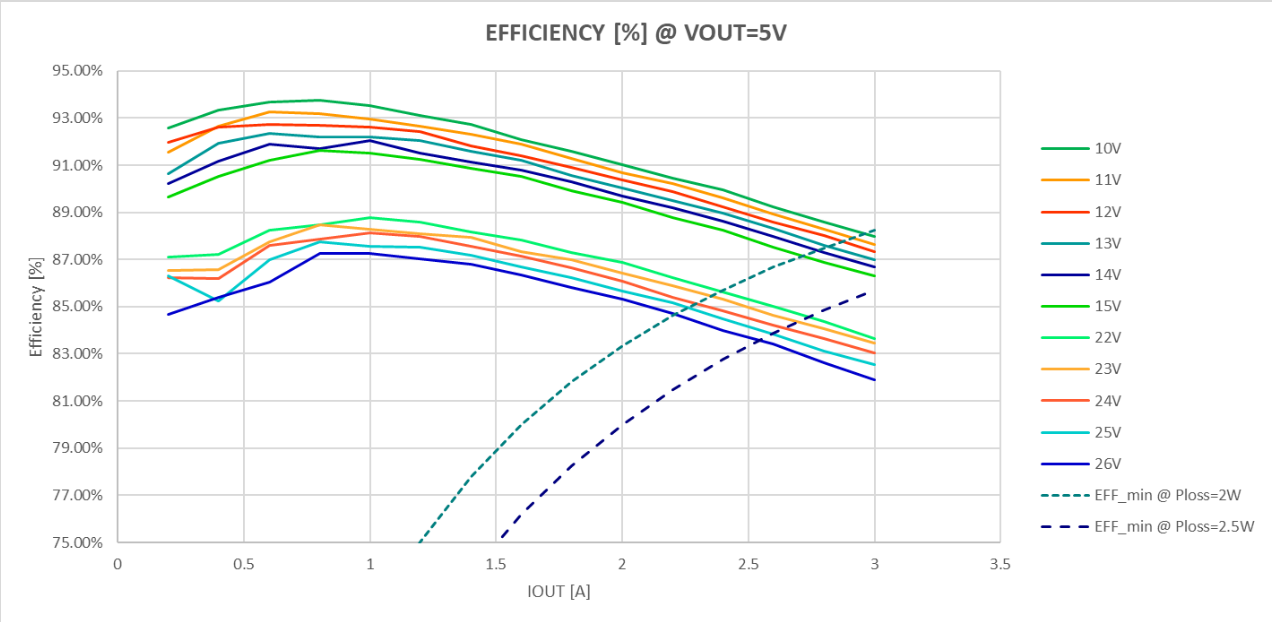



**Figure 10.** Efficiency η[%] vs. output current IOUT[A] at VOUT=5V selection and at different VIN[V]

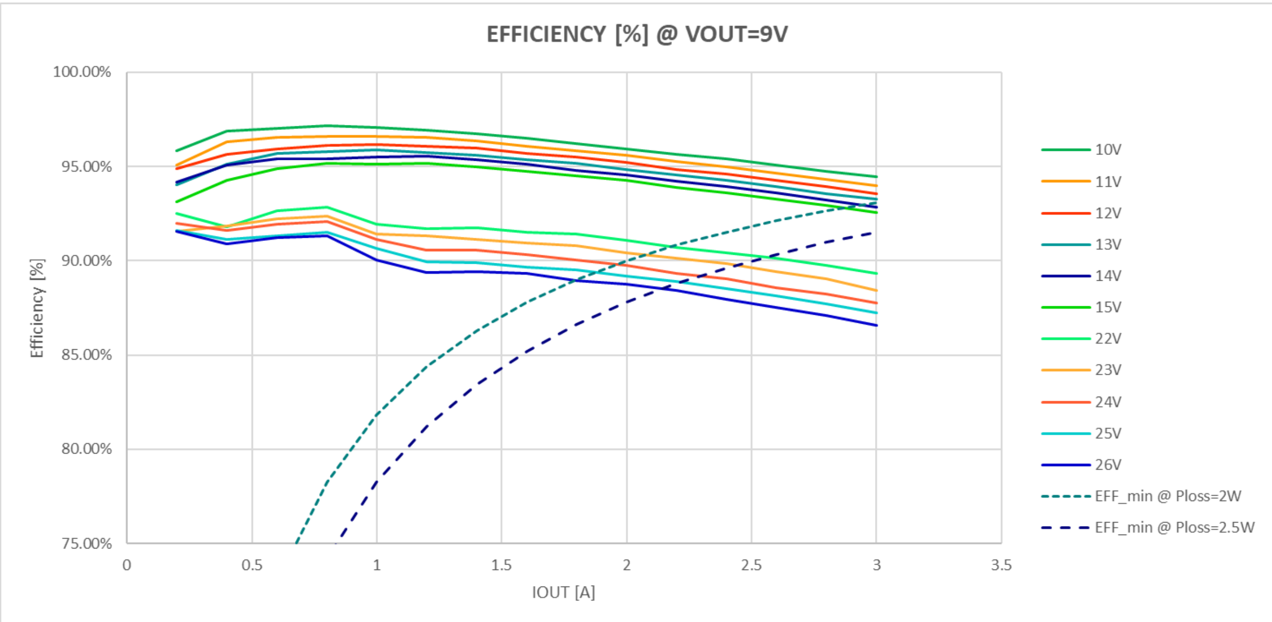



**Figure 11.** Efficiency η[%] vs. output current IOUT[A] at VOUT=9V selection and at different VIN[V]

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (continued)

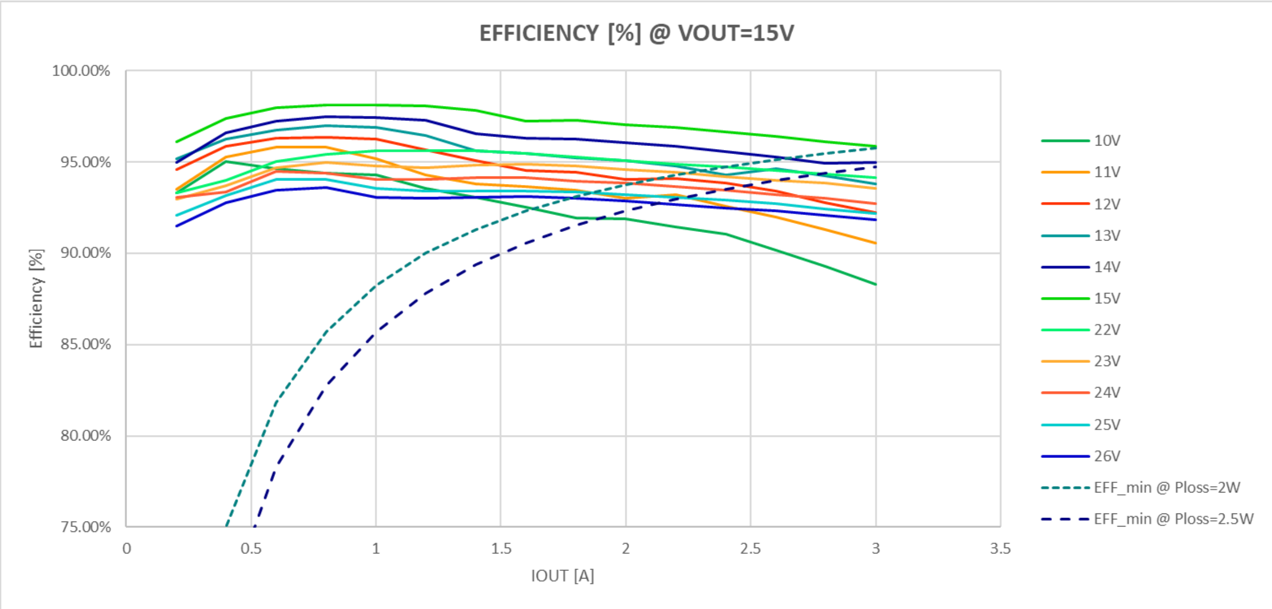



**Figure 12.** Efficiency η[%] vs. output current IOUT[A] at VOUT=15V selection and at different VIN[V]

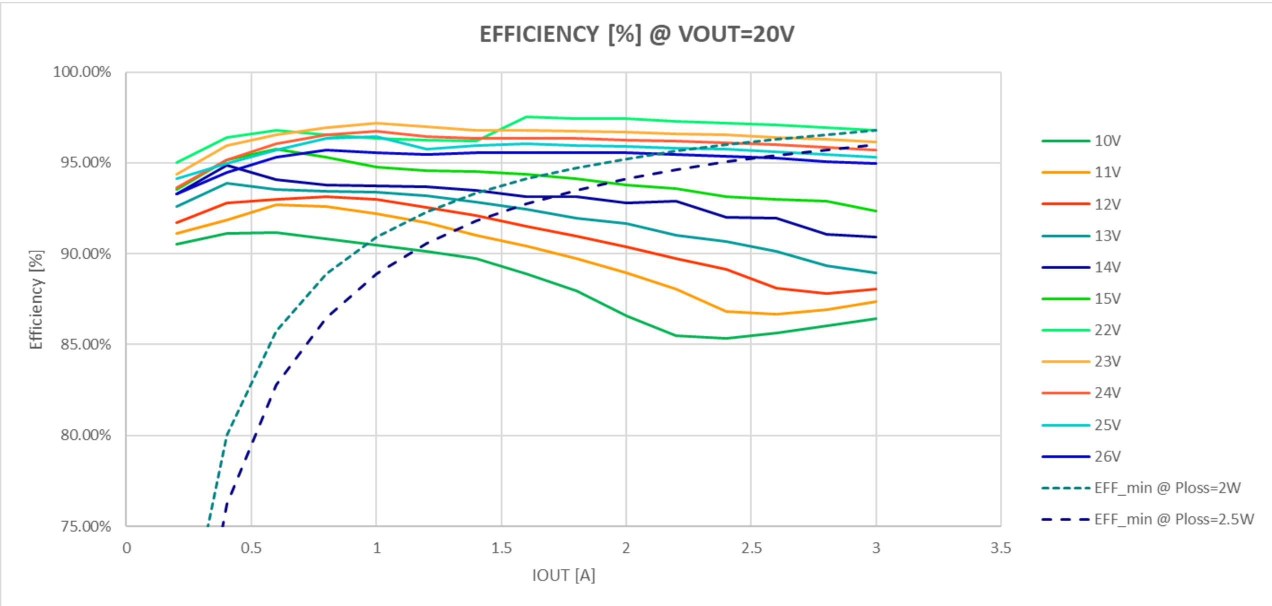



**Figure 13.** Efficiency η[%] vs. output current IOUT[A] at VOUT=20V selection and at different VIN[V]

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (continued)

**Power loss (heating power) (typical)**

Figures 14-17 present power losses at different input voltage VIN[V] and output current IOUT[V] conditions when output voltage VOUT[V] voltage is 5V, 9V, 15V and 20V. The dark green contour map represents power losses up to 2W and orange countour map corresponds to losses up to 2.5W.

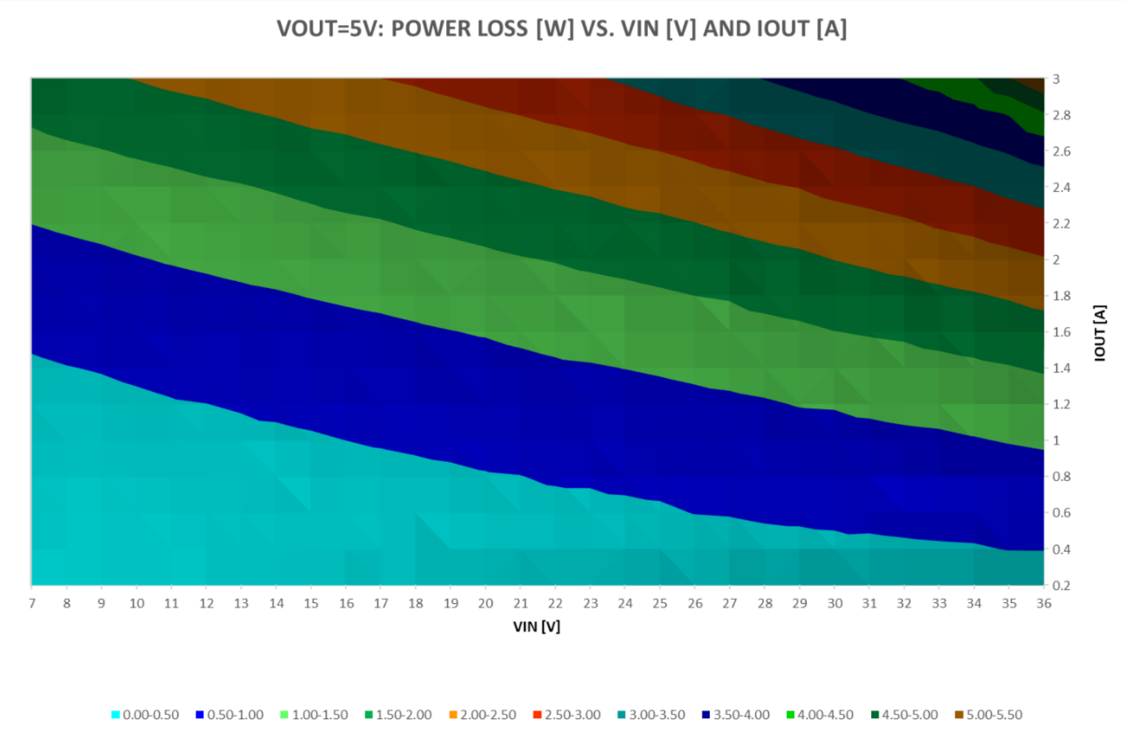



**Figure 14.** Power loss Ploss[W] vs. output current IOUT[A] at VOUT=5V selection and at different VIN[V]

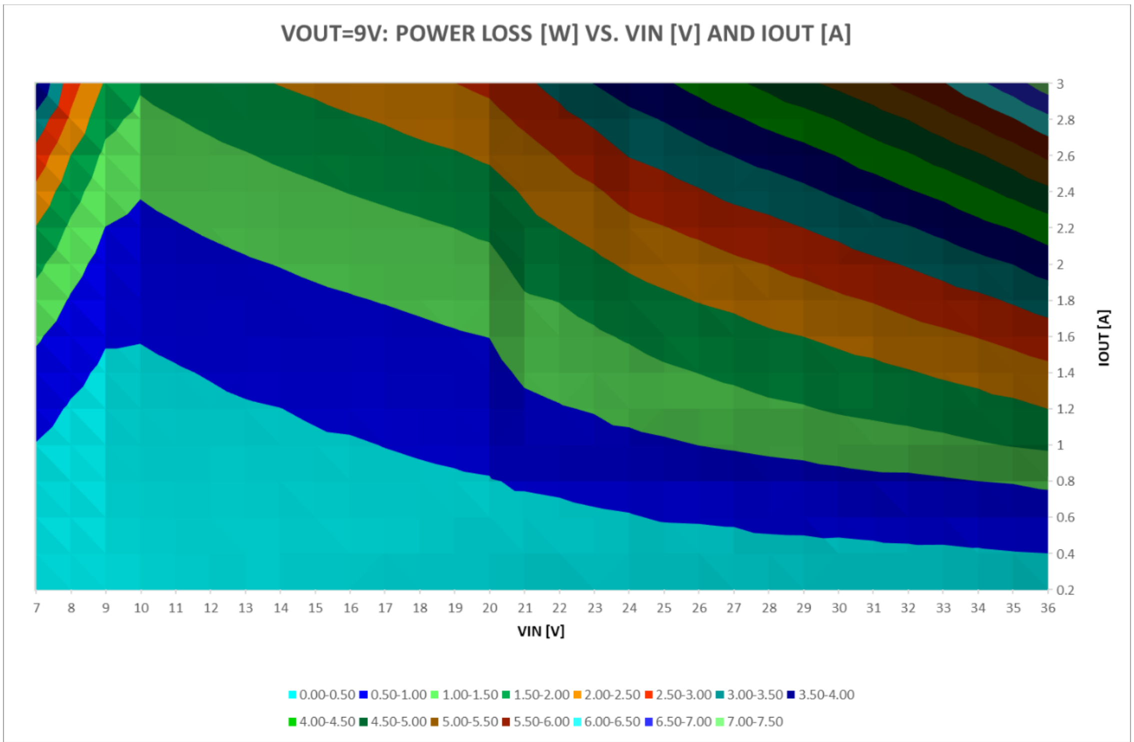



**Figure 15.** Power loss Ploss[W] vs. output current IOUT[A] at VOUT=9V selection and at different VIN[V]

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (continued)

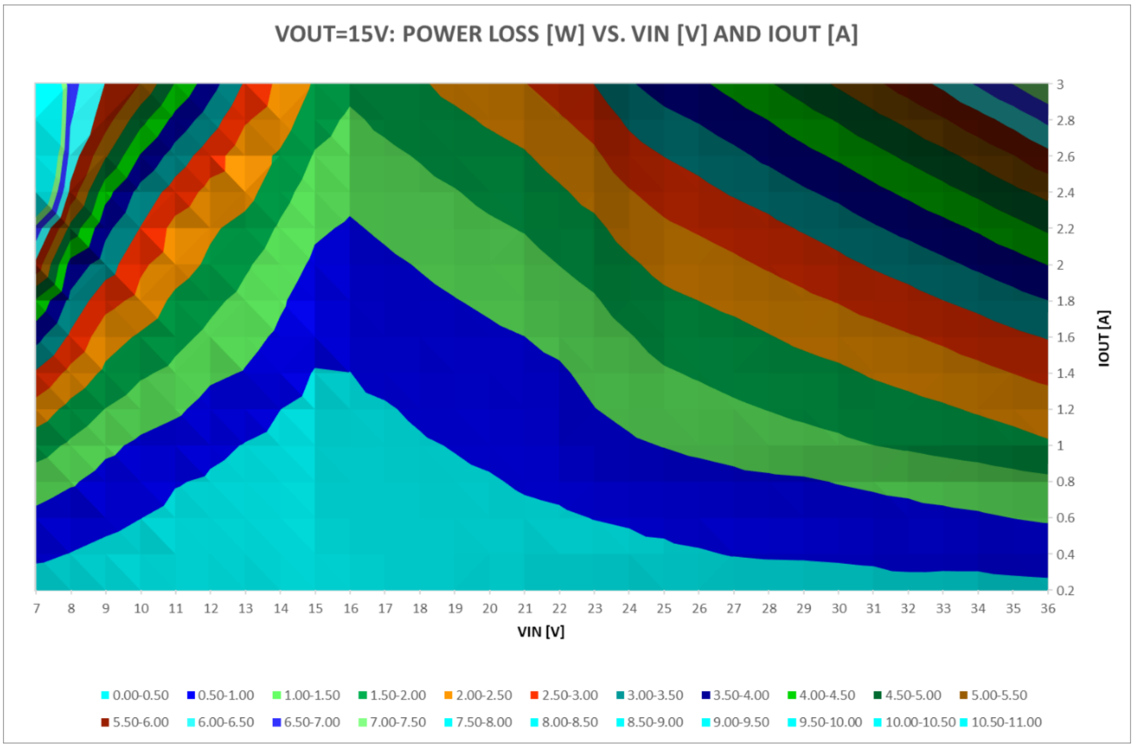



**Figure 16.** Power loss Ploss[W] vs. output current IOUT[A] at VOUT=15V selection and at different VIN[V]

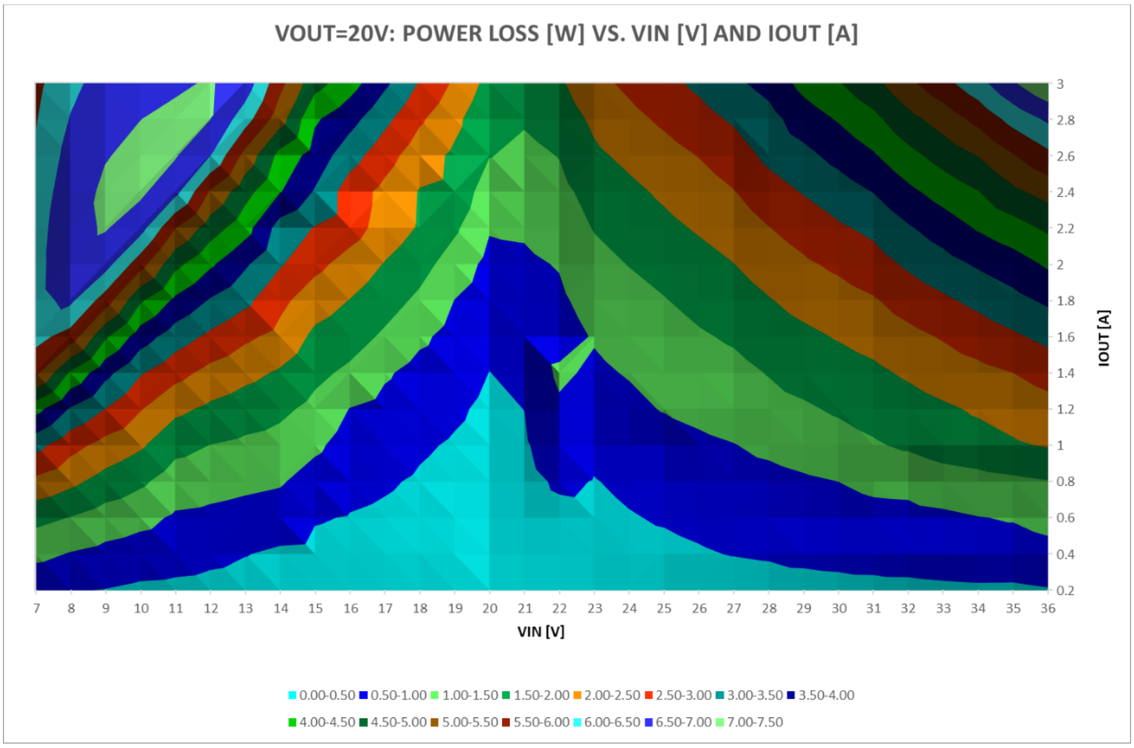
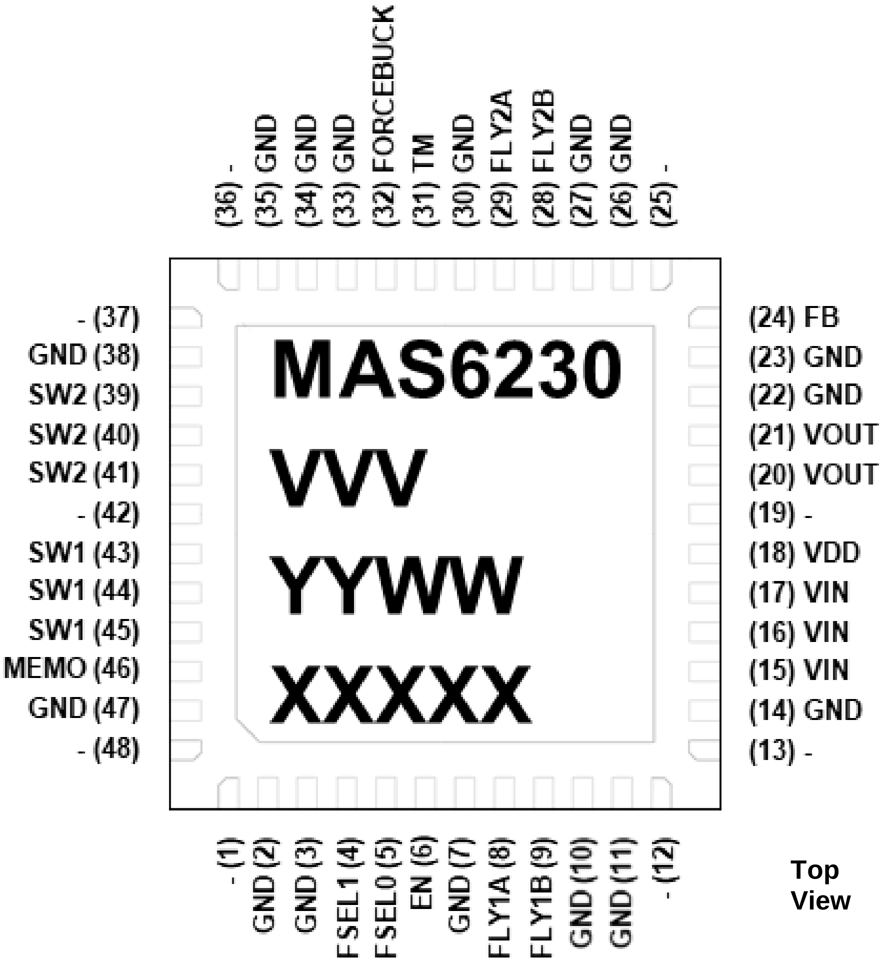



**Figure 17.** Power loss Ploss[W] vs. output current IOUT[A] at VOUT=20V selection and at different VIN[V]

## DEVICE OUTLINE CONFIGURATION




**Top Marking Information:**
**MAS6230 = Product**
**VVV = Version**
**YY = Year**
**WW = Week**
**XXXXX = Lot number**

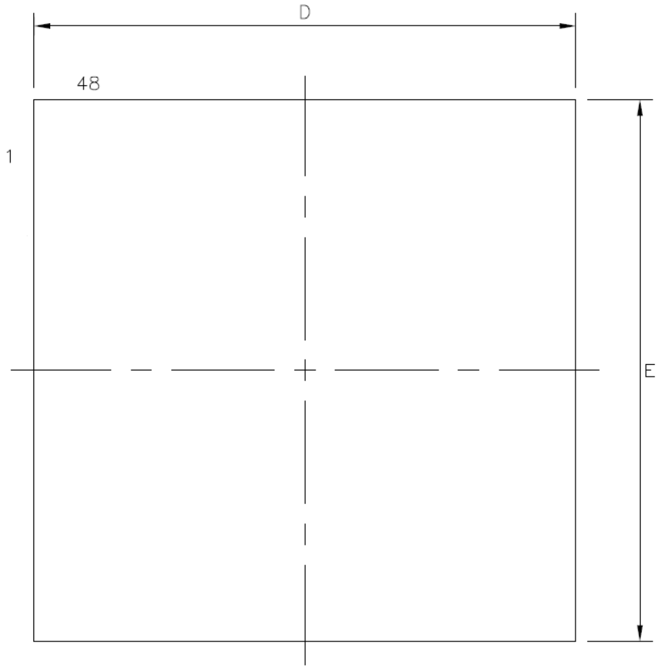
**Top View**

## QFN-48 7x7x0.75 PIN DESCRIPTION

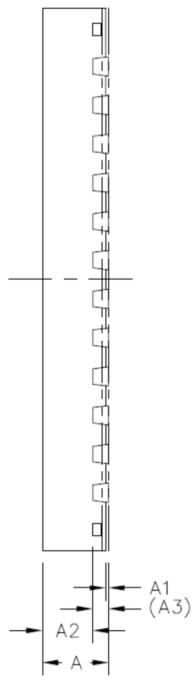
| Parameter | Unit | Value | Note | |
|---|---|---|---|---|
| **Pin Name** | **Pin** | **Type** | **Function** | **Note** |
| - | 1 | - | Not connected | 1 |
| GND | 2-3 | G | Ground | |
| FBSEL1 | 4 | DI | Output voltage selection bit 1 | |
| FBSEL0 | 5 | DI | Output voltage selection bit 0 | |
| EN | 6 | DI | DC/DC enable | |
| GND | 7 | G | Ground | |
| FLY1A | 8 | AO | Flying capacitor 1 positive terminal | |
| FLY1B | 9 | AO | Flying capacitor 1 negative terminal | |
| GND | 10-11 | G | Ground | |
| - | 12-13 | - | Not connected | 1 |
| GND | 14 | G | Ground | |
| VIN | 15-17 | P | DC/DC Input voltage | |
| VDD | 18 | AO | Internal power supply | |
| - | 19 | - | Not connected | 1 |
| VOUT | 20-21 | AO | DC/DC output voltage | |
| GND | 22-23 | G | Ground | |
| FB | 24 | AI | Feedback | |
| - | 25 | - | Not connected | 1 |
| GND | 26-27 | G | Ground | |
| FLY2B | 28 | AO | Flying capacitor 2 negative terminal | |
| FLY2A | 29 | AO | Flying capacitor 2 positive terminal | |
| GND | 30 | G | Ground | |
| TM | 31 | DIO | Test mode pin | 2 |
| FORCEBUCK | 32 | DI | Force Buck selection<br>Buck operation: FORCEBUCK=VDD<br>Buck/boost operation: FORCEBUCK=GND | 3 |
| GND | 33-35 | G | Ground | |
| - | 36-37 | - | Not connected | 1 |
| GND | 38 | G | Ground | |
| SW2 | 39-41 | AO | Inductor switch terminal 2 | |
| - | 42 | - | Not connected | 1 |
| SW1 | 43-45 | AO | Inductor switch terminal 1 | |
| MEMO | 46 | AI | Memory test input | 2 |
| GND | 47 | G | Ground | |
| - | 48 | - | Not connected | 1 |

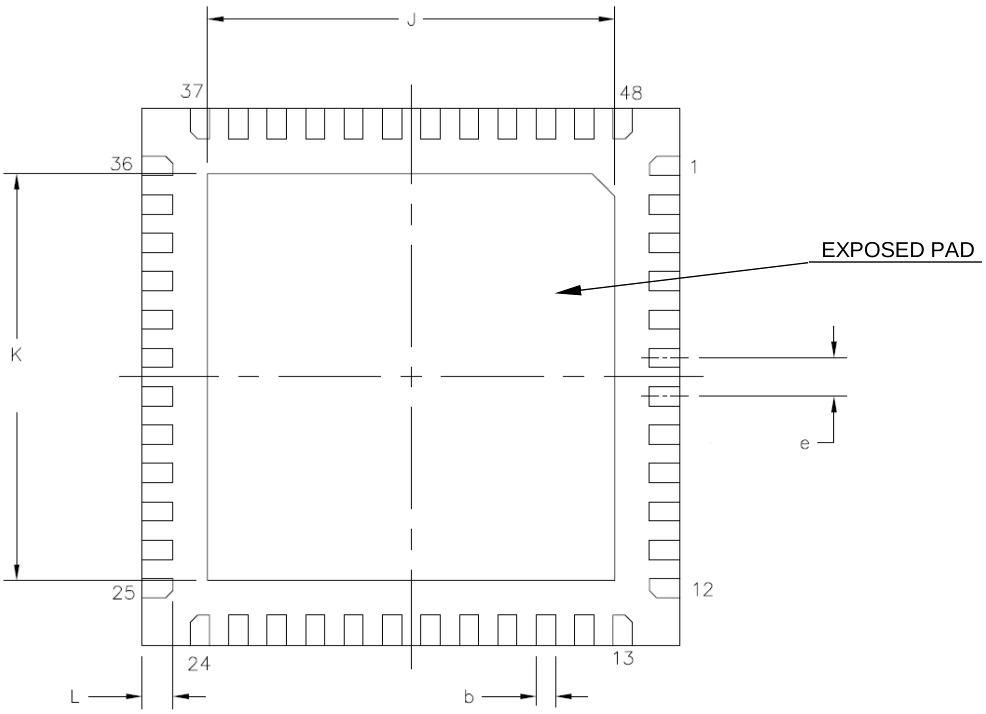
G = Ground, P = Power, D = Digital, A = Analog, I = Input, O = Output
**Note 1:** Not connected pins should be connected to ground
**Note 2:** The TM and MEMO pins are only for internal testing purpose and must be connected to GND in the application
**Note 3:** In applications which require only buck operation ($V_{IN} > V_{OUT}$) the FORCEBUCK is connected to VDD pin. This forces device into buck operation by disabling boost operation ($V_{IN} < V_{OUT}$). In other applications the FORCEBUCK is connected to GND. This enables both buck and boost operations.
**Note:** Thermal pad (exposed pad) must be connected to continuous ground plane(s) using thermal vias to guarantee maximal heat transfer

## PACKAGE (QFN-48 7x7x0.75) OUTLINE




TOP VIEW




BOTTOM VIEW

## PACKAGE (QFN-48 7x7x0.75) OUTLINE (continued)

| Symbol | Min | Nom | Max | Unit |
|---|---|---|---|---|
| PACKAGE DIMENSIONS | | | | |
| A | 0.7 | 0.75 | 0.8 | mm |
| A1 | 0 | 0.035 | 0.05 | mm |
| A2 | --- | 0.55 | 0.57 | mm |
| A3 | | 0.203 REF | | mm |
| b | 0.2 | 0.25 | 0.3 | mm |
| D | | 7 BSC | | mm |
| E | | 7 BSC | | mm |
| e | | 0.5 BSC | | mm |
| J (Exposed.pad) | 5.2 | 5.3 | 5.4 | mm |
| K (Exposed.pad) | 5.2 | 5.3 | 5.4 | mm |
| L | 0.35 | 0.4 | 0.45 | mm |

## ORDERING INFORMATION

| Product Code | Product | Package | Comments |
|---|---|---|---|
| MAS6230BA1Q2406 | High Efficiency 60W Buck-Boost DC/DC Converter | QFN-48 7x7x0.75, Pb-free, RoHS compliant | Tape and Reel 3000 pcs / r |

## LOCAL DISTRIBUTOR

## MICRO ANALOG SYSTEMS OY CONTACTS

| | |
|---|---|
| Micro Analog Systems Oy<br>Kutomotie 16<br>FI-00380 Helsinki, FINLAND | Tel. +358 10 835 1100<br><br>http://www.mas-oy.com |