MAS6279D8

IC FOR 5.00 – 64.00 MHz VCTCXO

- **Fifth Order Compensation**
- **Frequency Stability ± 0.10 ppm**
- **Wide Frequency Range**
- **Very Low Phase Noise**
- **Minimum Operating Temperature –40 °C**
- **EEPROM Selectable Output**
- **Tri State Output**

DESCRIPTION

The MAS6279D8 is an integrated circuit well suited to build high end VCTCXO for telecommunication. The trimming is done through a serial bus and the calibration information is stored in an internal EEPROM.

To build a VCTCXO only a crystal is required in addition to MAS6279D8. The compensation method is fully analog, working continuously without generating any steps or other interference.

FEATURES

- Very small size
- Minimal current consumption
- Wide operating temperature range
- Very low phase noise
- Minimum operating temperature –40 °C
- Oscillator frequency output selectable by EEPROM direct or $f_{XTAL}/2$.
- Output waveform selectable by EEPROM: clipped sine wave or CMOS.
- Possibility to use just a compensation part

APPLICATIONS

- (VC)TCXO for high end telecommunications systems
- (VC)TCXO for GPS
- (VC)TCXO for Stratum
- (VC)TCXO for Picocell
- (VC)TCXO for Femtocell

BLOCK DIAGRAM

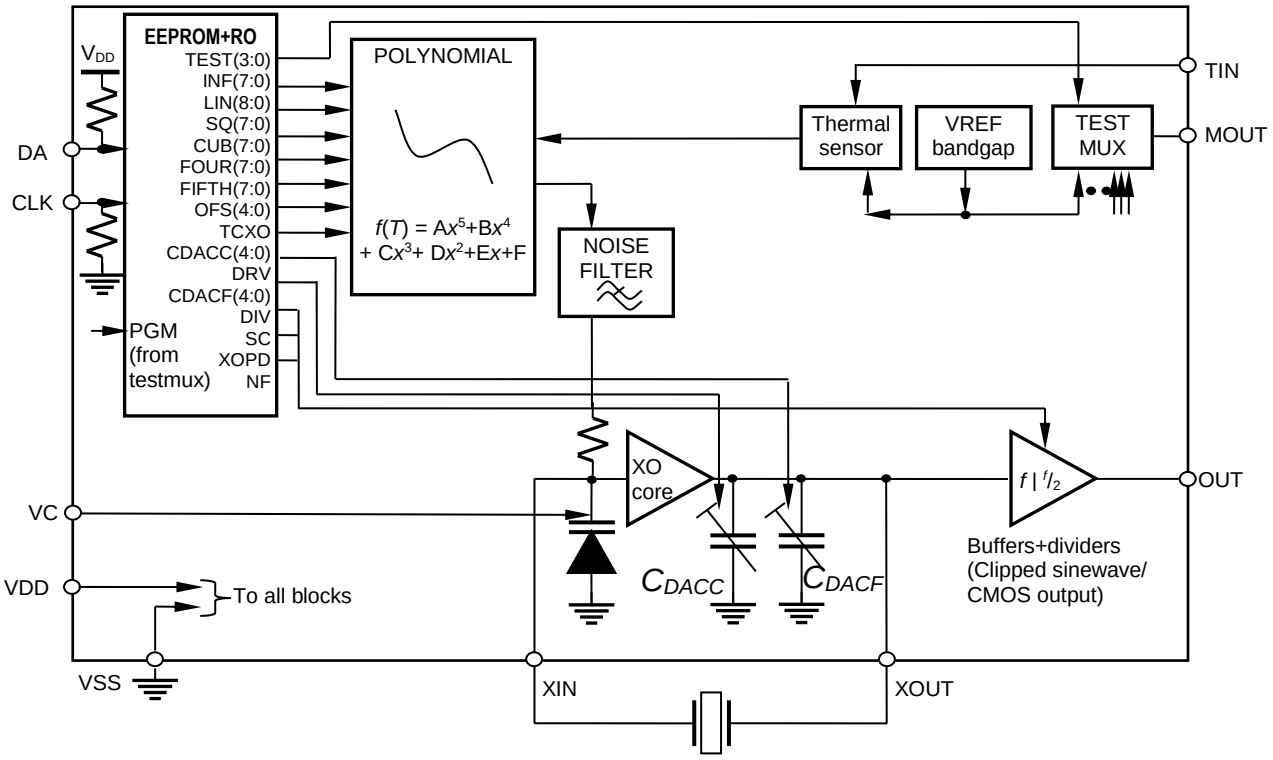


Figure 1. Block diagram of MAS6279D8.

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit	Note
Supply Voltage	V_{DD}		-0.3	5.0	V	
Voltage Range for All Pins	V_{IN}		-0.3	V_{DD} +0.3	V	
Latchup Current Limit	I_{LUT}	For all pins, test according to JESD78A.	-100	+100	mA	
Junction Temperature	$T_{J\ max}$			+150	°C	
Storage Temperature	T_S		-55	+125	°C	1)
ESD Rating		Human Body Model (HBM)		±1	kV	

Note 1: See EEPROM memory data retention at hot temperature. Storage or bake at hot temperatures will reduce data retention time of programmed EEPROM bits.
Note: The absolute maximum rating values are stress ratings only. Functional operation of the device at conditions between maximum operating conditions and absolute maximum ratings is not implied. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions above absolute maximum ratings may be destructive to the devices.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

RECOMMENDED OPERATION CONDITIONS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.6	3.3	3.6	V	
Supply Voltage at EEPROM Programming	V_{DD}	T=+25°C	3.0	3.3	3.6	V	1)
Operating Temperature	T_A		-40	+25	+85	°C	
Crystal Pulling Sensitivity	S	C_L=7.2pF		37		ppm/pF	
Crystal Load Capacitance	C_L	VC = 1.65V		7.2		pF	
Crystal Rs	Rs			20	50	Ω	

Note 1**:** The recommended condition for EEPROM programming is room temperature.
Note: The device performance may deteriorate in the long run if the Recommended Operation Conditions limits are continuously exceeded.

ELECTRICAL CHARACTERISTICS

(recommended operating conditions)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
EEPROM size				70		bit	
EEPROM data retention		T_A = +85 °C T_A = +125 °C	10	24 1		years	
Serial Bus (DA/CLK) Clock Frequency	f_{CLK}				100	kHz	
Input High Voltage (DA/CLK)	V_{IH}		80% VDD		100% VDD	V	
Input Low Voltage (DA/CLK)	V_{IL}		0% VDD		20% VDD	V	

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, VDD = 2.6V to 3.6V, Typ T_A = 25°C, Typ VDD = 3.3 V, Typ VC = 1.65 V, f_{XTAL} = 26MHz unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Crystal Frequency Range	f_{XTAL}		10.00		64.00	MHz	1)
Output Frequency Range	f_o		5.00		64.00	MHz	1)
Voltage Control Range	VC		0	1.65	V_{DD}	V	2)
Voltage Control Sensitivity	VC_{SENS}			5		ppm/V	3)
Voltage Control Linearity	VC_{LIN}			±10		%	4)
Frequency vs. Supply Voltage, Clipped Sinewave Output	df_o	V_{DD} ± 5%			±0.1	ppm	5)
Frequency vs. Supply Voltage, CMOS Output	df_o	V_{DD} ± 5%			±0.1	ppm	5)
Frequency vs. Load Change	df_o				±0.1	ppm	6)
Output Voltage (10 kΩ || 10 pF)	V_{out}		0.8	1.0		Vpp	7)
Output Voltage (15 pF)	V_{out}				V_{DD}	Vpp	8)
Output Voltage Levels	VOH_{OUT}		0.8*V_{DD}		V_{DD}		8)
	VOL_{OUT}		0		0.2*V_{DD}		8)
Rise and Fall Time				3		ns	8)
Duty Cycle			40	50	60	%	
Supply Current, Clipped Sinewave Output	I_{DD}	10 MHz 26 MHz 40 MHz 52.5 MHz	0.9	1.3 2.0 2.5 2.7	2.8	mA	
Supply Current, CMOS Output	I_{DD}	10 MHz 26 MHz 40 MHz 52.5 MHz	1.6	1.8 2.8 4.1 6.3	3.6	mA	
Compensated Frequency Stability Over Temperature	df_o	-40 °C …+85 °C -20 °C …+70 °C 0 °C …+60 °C			±0.28 ±0.14 ±0.10	ppm	9)
Compensation Range Linear Part	a_1		-0.6	-0.37	-0.1	ppm/K	
Compensation Range Inflection Point	INF		20	28	36	°C	
Compensation Range Cubic Part	a_3			105		$10^{-12}/K^3$	
Amplitude Start up Time	T_{START}			2		ms	
Tri State Output Control Input Output OFF State (High-Z) Output ON State	 VIL_{DA} VIH_{DA}	DA pin voltage DA LOW DA HIGH	 0 V_{DD}-0.6		 0.55 V_{DD}	V	

Note 1: Frequency division by two is selected by EEPROM bit DIV: 0=no division, 1=div by 2. Thus output frequency range is 5-64 MHz.
Note 2: If VC is not needed, it should be left unconnected (floating) and TCXO bit set TCXO=1.
Note 3: Depending on a crystal pulling
Note 4: VC=1.65V ± 1.0V, V_{DD}=3.3V
Note 5: With divider
Note 6: Clipped sinewave output: 10 kΩ || 10 pF ± 10%. CMOS output: 15 pF ± 10%
Note 7: Clipped sinewave output only
Note 8: CMOS output only
Note 9: With proper crystals

ELECTRICAL CHARACTERISTICS

T_A = -40ºC to +85ºC, VDD = 2.6V to 3.6V, Typ T_A = 25ºC, Typ VDD = 3.3 V, Typ VC = 1.65 V, f_{XTAL} = 26MHz unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Phase Noise	φn CLIPPED SINEWAVE	@ 1Hz @ 10Hz @ 100Hz @ 1kHz @ 10kHz @ 100kHz		-57 -83 -113 -138 -148 -152		dBc/Hz	1)
	φn CMOS	@ 1Hz @ 10Hz @ 100Hz @ 1kHz @ 10kHz @ 100kHz		-62 -82 -113 -139 -149 -153		dBc/Hz	1)
	φn CLIPPED SINEWAVE + DIVIDER	@ 1Hz @ 10Hz @ 100Hz @ 1kHz @ 10kHz @ 100kHz		-56 -88 -118 -135 -145 -151		dBc/Hz	1)
	φn CMOS + DIVIDER	@ 1Hz @ 10Hz @ 100Hz @ 1kHz @ 10kHz @ 100kHz		-62 -89 -119 -135 -146 -152		dBc/Hz	1)

Note 1: Not measured in production testing

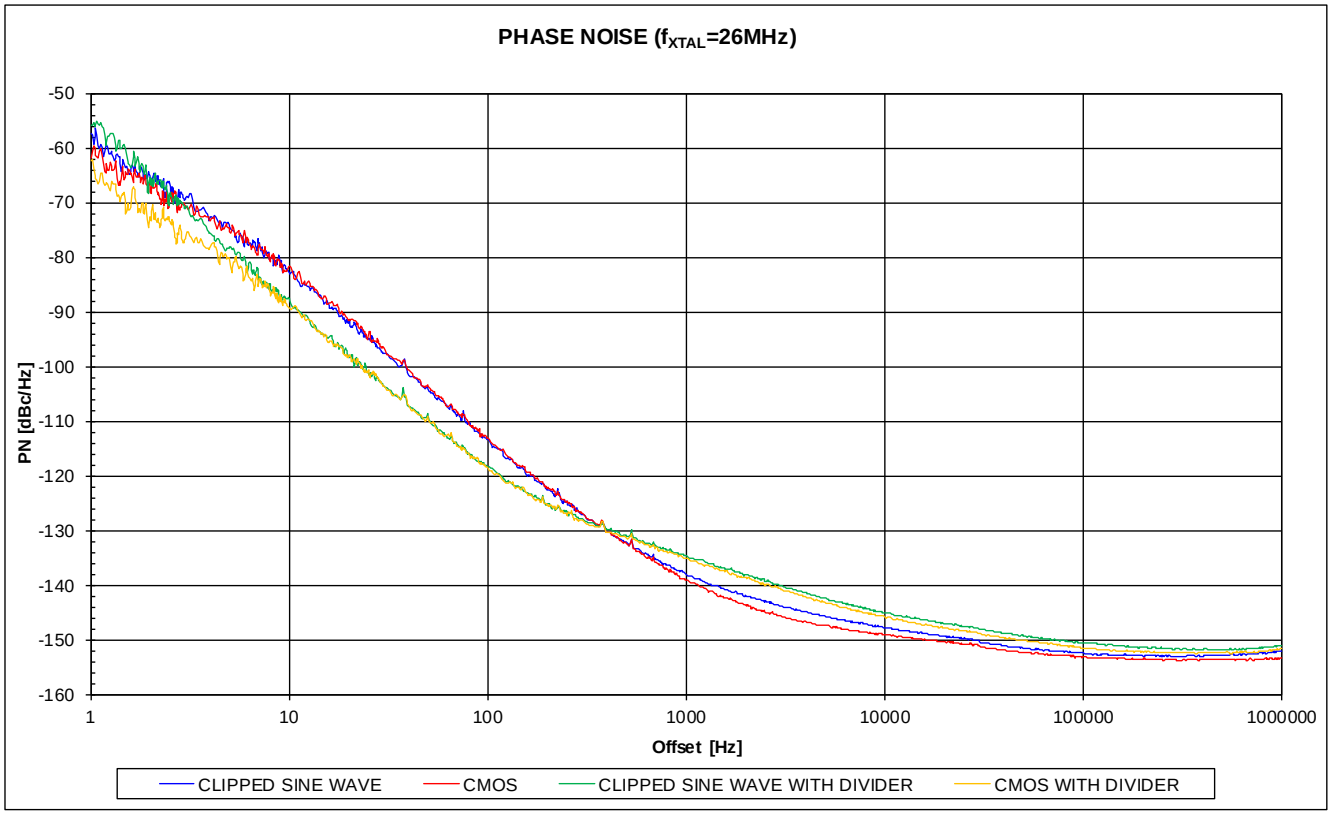


Figure 2. Phase noise with 26MHz crystal at clipped sinewave / CMOS output and without / with divider

RECOMMENDED CRYSTAL TEMPERATURE CHARACTERISTIC

Crystal cut angle determines crystal's temperature characteristic. The cut angle can be selected to minimize crystal's temperature dependency in the temperature range of interest. Table 1 below shows theoretical AT-cut crystal cut angles minimizing crystal batch temperature dependency at five different temperature ranges. In the optimization calculations the inflection temperature of the crystal has been +29°C and cut angle control tolerance ±0.12'. The cut angle values are in angular minutes (1'=1/60th of 1°) relative to AT-cut crystal angle 35° 15'.

Table 1. AT-cut crystal cut angles to minimize crystal's temperature dependency

Temperature range	AT crystal cut angle	Nominal crystal's temperature dependency
0°C…+60°C	1.13'	±1.1ppm (2.2ppm p-p)
-10°C…+60°C	1.70'	±2.1ppm (4.2ppm p-p)
-20°C…+70°C	2.55'	±3.8ppm (7.6ppm p-p)
-30°C…+85°C	3.57'	±6.3ppm (12.6ppm p-p)
-40°C…+85°C	4.77'	±9.7ppm (19.8ppm p-p)

Figure 3 below illustrates theoretical temperature characteristic of above five cut angle crystals for different temperature ranges. The widest temperature range -40°C…+85°C requires largest cut angle and the narrowest temperature range 0°C…+60°C smallest cut angle.

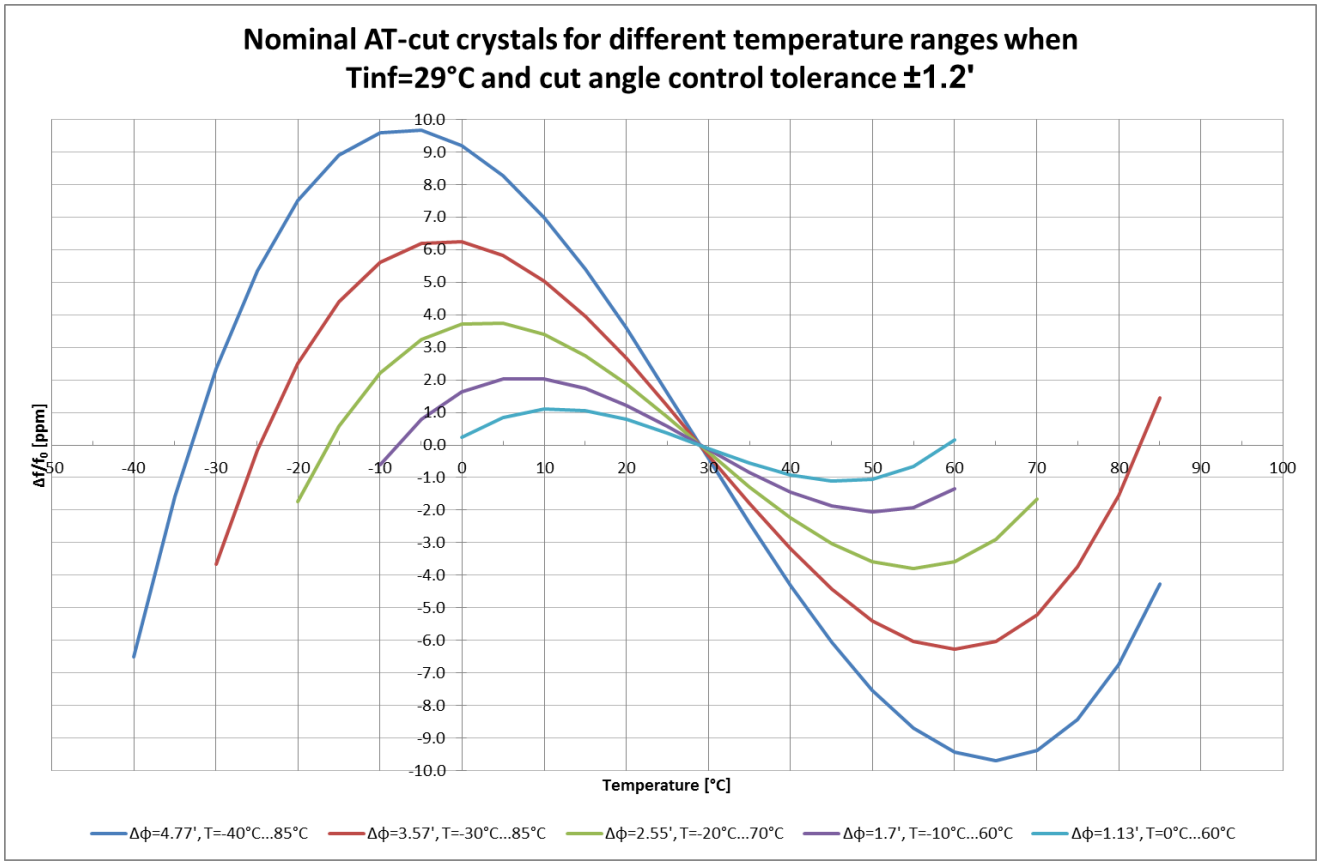
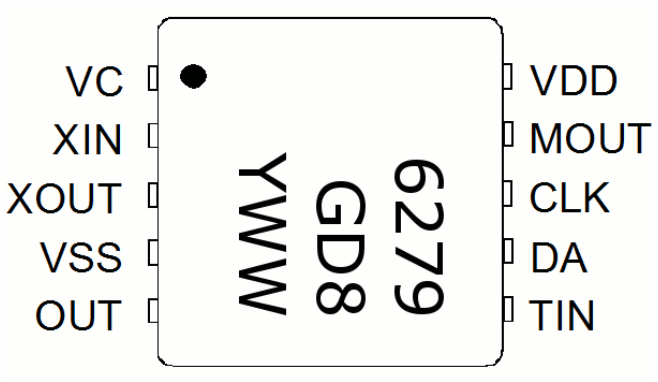


Figure 3. Temperature characteristic of five AT-cut crystals with different cut angles

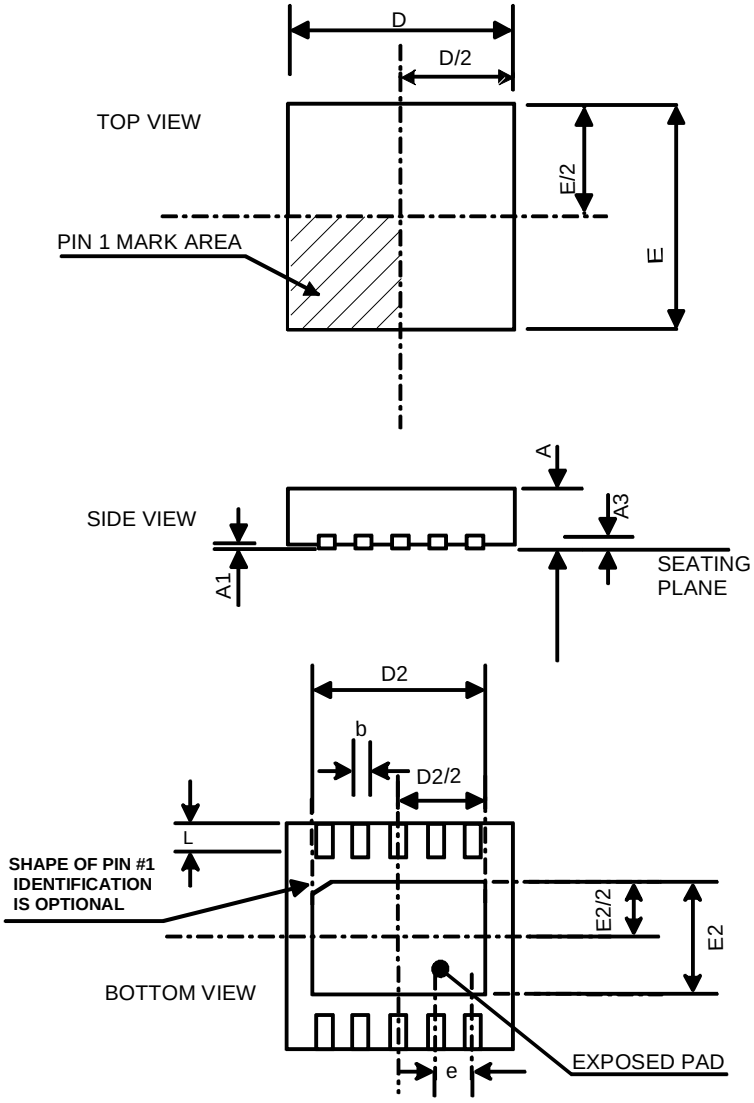
DEVICE OUTLINE CONFIGURATION

DFN-10 3 x 3 x 0.75



G = Green
D8 = Version
Y = Year
WW = Week

PACKAGE (DFN-10 3x3x0.75) OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3	0.178	---	0.228	mm
b	0.200	---	0.300	mm
D	2.950	3.000	3.050	mm
D2 (Exposed.pad)	2.500	---	2.700	mm
E	2.950	3.000	3.050	mm
E2 (Exposed.pad)	1.650	---	1.750	mm
e		0.500 BSC		mm
L	0.350	---	0.450	mm

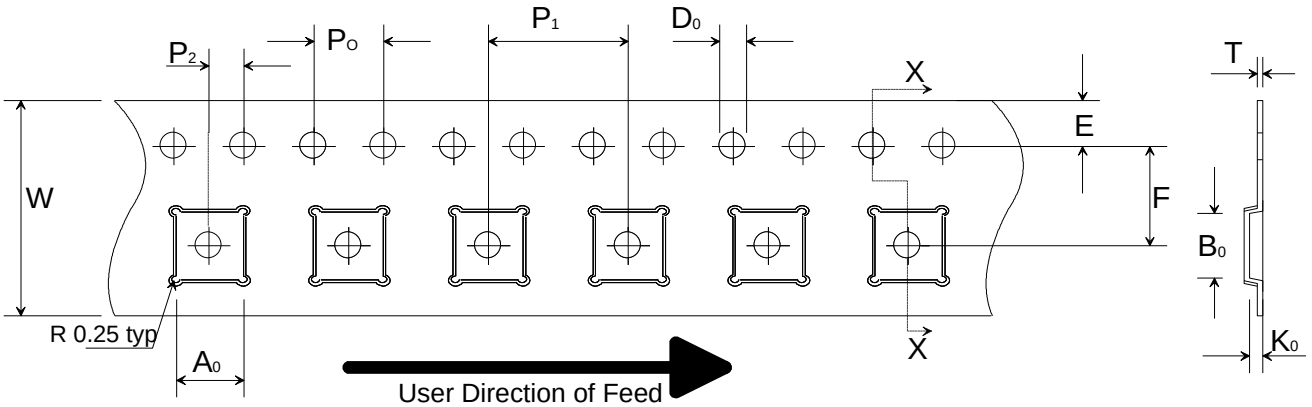
Dimensions do not include mold or interlead flash, protrusions or gate burrs.

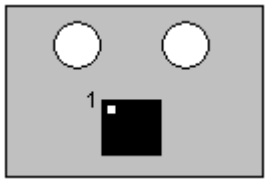
SOLDERING INFORMATION

◆ **For Lead-Free / Green DFN 3mm x 3mm x 0.75mm**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	7.62 - 25.4 µm, Matte Tin

EMBOSSED TAPE SPECIFICATIONS



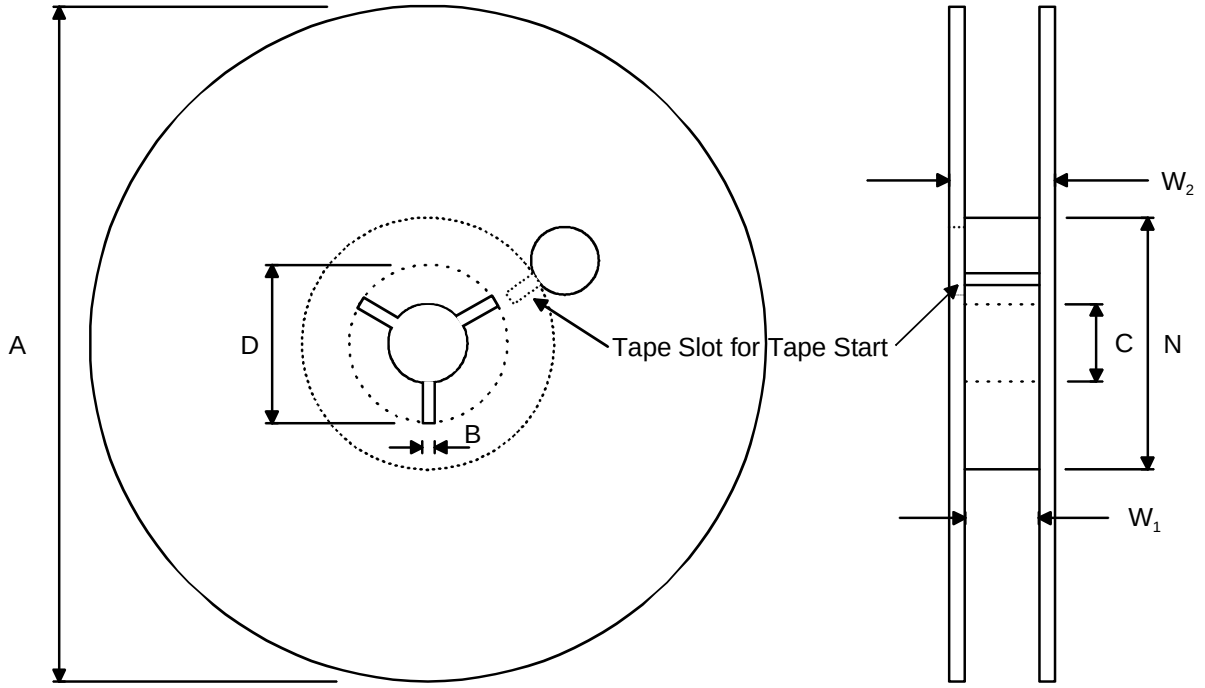


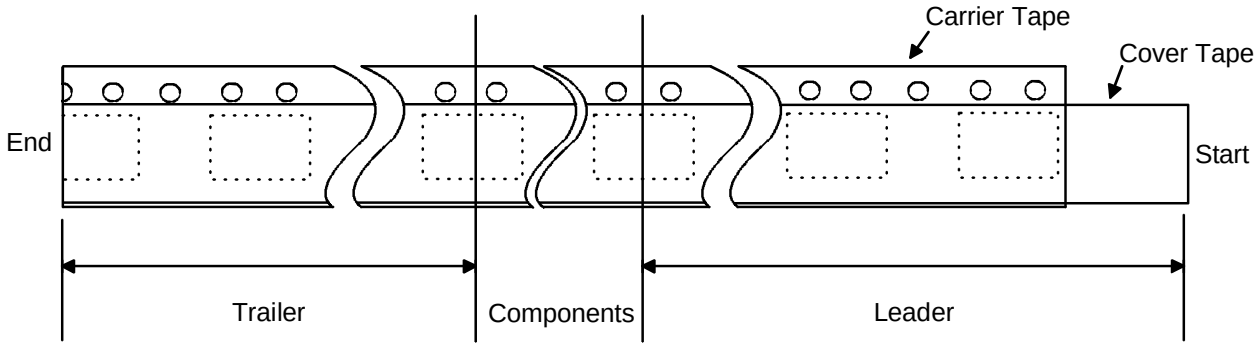
Orientation on tape

Dimension	Min/Max	Unit
Ao	3.30 ±0.10	mm
Bo	3.30 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
Ko	1.10 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

All dimensions in millimeters

REEL SPECIFICATIONS





Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	100		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

3000 Components on Each Reel
Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Package
MAS6279D8WAD00	IC for VCTCXO	Tested wafer, thickness 370 µm
MAS6279D8WAB05	IC for VCTCXO	Tested 180 µm thick bare die on tray
MAS6279D8HP06	IC for VCTCXO	DFN-10 3x3x0.75, T&R 3000 pcs / reel, Pb free RoHS

Contact Micro Analog Systems Oy for other wafer and die thickness options.

◆ **Product code details**

Product name	Design version	Package type	Delivery format
MAS6279	D8	WAB = 180 µm thick tested wafer or bare die WAD = 370 µm thick tested wafer or bare die HP = DFN-10 3x3x0.75 mm	00 = tested wafer 05 = die tray 06 = T&R 3000 pcs

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

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DOCUMENT VERSION HISTORY

000	Initial version
001	On page 3 nominal crystal load capacitance (C_L) of MAS6279D8 corrected from 8pF to 7.2pF. Crystal pulling sensitivity (S) changed from 32ppm/pF to 37ppm/pF.