MAS6510

Capacitive Sensor Signal Interface IC

- **Single or Dual Capacitance Sensors**
- **Very Low Power Consumption**
- **On Chip Temperature Sensor**
- **VDD Level Monitoring**
- **24-Bit Ratiometric ΔΣ CDC**
- **EEPROM Calibration Memory**
- **SPI or I2C Bus with programmable I2C device address**

DESCRIPTION

MAS6510 capacitive sensor signal Interface IC can interface both single and dual capacitance sensors.

It uses a 24-bit Capacitance-to-Digital Converter (CDC), which employs a delta-sigma (ΔΣ) conversion technique. The output data from the high order ΔΣ-modulator is processed by an on-chip decimator filter, producing a high resolution conversion result. The converter is run by an internal clock oscillator making an external converter clock unnecessary.

The converter input range is programmable to meet various sensor offset and changing capacitance values. Maximum sensor capacitance is 40pF but higher maximum value can be reached by using slower conversion speed or scaling the signal by using an external series capacitor.

The measurement resolution depends on the programmed capacitance range and over sampling ratio (OSR) selections.

MAS6510 supports two capacitance measurement modes. The output can be proportional either to capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S.

The IC is designed especially to meet the requirement for low power consumption, thus making it an ideal choice for battery powered systems. Current consumption values of 47.9 µA with high resolution or 3.3 µA with low resolution, at a conversion rate of one conversion per second, can be achieved.

In addition to measuring capacitance the device has an internal temperature sensor for temperature measurement and temperature compensation purposes. The VDD level monitoring feature is useful especially in battery operated systems. The 256-bit EEPROM memory stores trimming and calibration coefficients on chip.

A serial interface, compatible with a bi-directional 2-wire I2C bus and 4-wire SPI bus, is used for conversion setup, starting a conversion and reading the conversion result.

FEATURES

- Sensor Offset and Gain Adjustment
  - Changing Capacitance Range ΔC 2pF…30pF
  - Internal Offset Capacitance Matrix 0pF…22pF
  - External Capacitance up to 40pF (or higher using external clock)
- Resolution 17.5 bit
- Internal Clock Oscillator
- On Chip Temperature Sensor -40°C...+85°C
- VDD Level Monitoring
- Low Voltage Operation 1.8 V/1.9V…3.6 V
- Low Supply Current: 3.3 µA...47.9 µA
- Conversion Time 5.8ms...82.6ms (12Hz...173Hz)
- Internal 256-bit EEPROM Calibration Memory
- Internal Clock Oscillator
- I2C and SPI Compatible Serial Interface
- QFN-16 Package

APPLICATIONS

- Capacitive Pressure Sensors
- Humidity Sensors
- Medical Devices
- Flow Meters
- Sport Watches
- Altimeter and Barometer Systems
- Mobile and Battery Powered Systems
- Low Frequency Measurement applications
- Current/Power Consumption Critical Systems
- Industrial and Process Control applications in noisy environments

BLOCK DIAGRAM

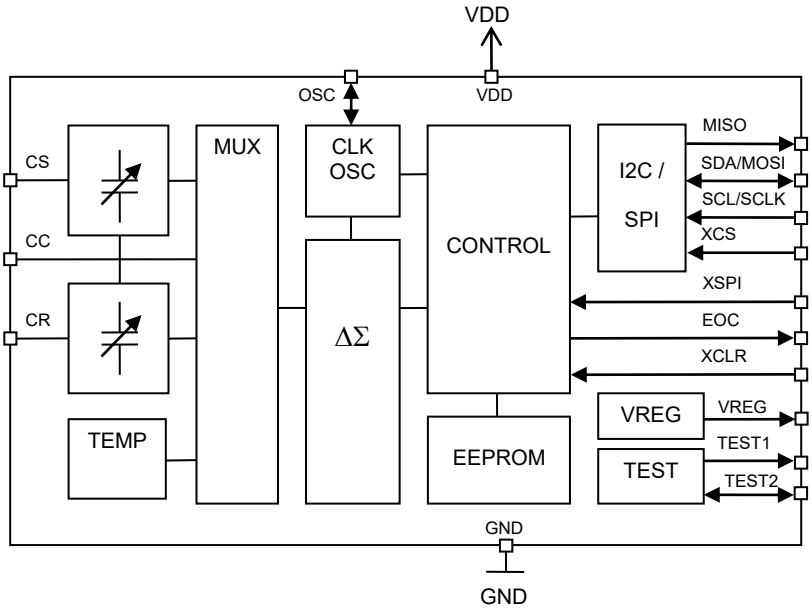


Figure 1. MAS6510 block diagram

FUNCTIONAL DESCRIPTION

MAS6510 can interface both single and dual capacitance sensors. Single capacitance sensors should be connected between the CS and the CC inputs. The second capacitor of a dual capacitance sensor should be connected between the CR and the CC inputs.

A Capacitance-to-Digital Converter (CDC) converts the input capacitances into a 24-bit output word (code). The converter front-end can be configured either for capacitance difference (C_S-C_R) or capacitance ratio (C_S-C_R)/C_S measurement mode. The ratio mode offers pre-linearization for sensor signals C_S(x) being proportional to ~1/x such as pressure sensor signals (x=pressure).

Converter resolution is selected by the over sampling ratio (OSR) setting. Higher OSR corresponds to higher resolution but also longer conversion time.

There are two internal 22pF capacitance matrices connected to the CS and the CR inputs. These matrices are used for sensor offset calibration and are programmable in 8-bit steps (86fF/step).

The gain is programmable with 8-bits resolution and sets the input range for sensor changing capacitance $\Delta C=C_{S\ MAX}-C_{S\_MIN}$.

MAS6510 includes an internal temperature sensor for temperature compensation purposes. A multiplexer in the front-end is used to select the external capacitive sensor, the internal temperature sensor or an internal band gap reference voltage in the VDD level monitoring mode.

Trim and calibration coefficients can be stored in the 256-bit EEPROM memory. In normal mode the stored trim values for the oscillator frequency, offset capacitance and gain are automatically read from the EEPROM memory in the beginning of each conversion. However by using Trimming control Register it is also possible to choose taking trimming values from the trimming registers instead of EEPROM.

To avoid modification of the EEPROM by mistake there is an EEPROM write enable bit in the EEPROM Control Register which needs to be set high (1) before any changes can be done to the EEPROM.

MAS6510 has an internal clock oscillator making an external clock unnecessary. To save power it's turned on only when a conversion is running. The frequency is factory trimmed to 200 kHz using a 6-bit register. An external clock, connected to the OSC pin, can however be used when a specific test mode is chosen. This may be necessary when measuring larger capacitances which require a slower clock frequency.

In temperature measurement mode it is necessary to always use a regulated supply voltage. This is achieved by enabling an internal 1.8V voltage regulator. When enabled the internal regulator is automatically turned on during conversion and off when conversion has been finished. Note that the internal regulator should be enabled only in the temperature measurement mode but kept disabled during capacitance and VDD monitoring modes.

FUNCTIONAL DESCRIPTION

In battery operated applications the VDD of the MAS6510 can vary along with battery capacity. In such case the VDD level monitoring feature can be useful to indicate battery level, help choosing between different power modes in the system or even using measured VDD level for compensating VDD dependencies. In the VDD level monitoring mode the on-chip regulator has to be disabled.

Communication with MAS6510 is handled by the serial interface compatible with either a bi-directional 2-wire I2C bus or a 4-wire SPI bus. The XSPI pin is for selecting which bus type is used.

Note: The 2-wire I2C bus of MAS6510 supports only basic I2C bus communication protocol but not for example 10-bit addressing, arbitration and clock stretching features of the I2C bus specification.

The XCLR pin can be used to hard reset the device including the serial communication. Device reset is possible also via serial bus using the reset register.

Connecting VDD triggers internal power on reset (POR) circuit which resets the device. However if the VDD rise time can exceed 1ms it is necessary keep the device in a reset during power up by the XCLR pin. Violating this may risk the EEPROM memory integrity. See APPLICATION INFORMATION for examples of external POR circuits.

Despite of on chip power on reset (POR) circuit it is recommended to reset the device manually after every power up to guarantee proper register settings after any VDD rise conditions.

The EOC pin indicates if a conversion has finished and the result is ready to be read from the memory via the serial interface. Using the EOC signal is not necessary since it is alternatively possible to wait at least maximum conversion time period before reading out the result.

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	5.0	V
Voltage Range for All Pins			-0.3	V_{DD} + 0.3	V
Latchup Current Limit	I_{LUT}	For all pins, test according to JESD78A.	-100	+100	mA
Junction Temperature	T_{Jmax}			+ 150	°C
Storage Temperature	T_S	Note 1	- 55	+125	°C

Note 1: See EEPROM memory data retention at hot temperature. Storage or bake at hot temperatures will reduce the wafer level trimming and calibration data retention time.
Note: The absolute maximum rating values are stress ratings only. Functional operation of the device at conditions between maximum operating conditions and absolute maximum ratings is not implied and EEPROM contents may be corrupted. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions above absolute maximum ratings may be destructive to the devices.
Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Capacitance and VDD level monitoring modes Note 1	1.8	2.7	3.6	V
		Temperature mode Note 1	1.9	2.7	3.6	V
Operating Temperature	T_A		-40	+25	+85	°C
EEPROM Write Temperature	T_A	Note 2	+10	+25	+40	°C

Note 1. In capacitance measurement and VDD level monitoring the regulator must be disabled (TEMPREGEN=0) which allows operation down to 1.8V. In temperature measurement the typ 1.8V regulator has to be enabled (TEMPREGEN=1) which limits the minimum supply voltage down to 1.9V.
Note 2: EEPROM write operation is recommended to be done at room temperature

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7V, T_A = -40°C to +85°C, Typ T_A = 27°C, SOSC=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal regulator voltage	VREG	Temp mode regulator enabled Note 1.	1.75	1.8	1.85	V
Standby current	I_{STBY}	All inputs at VDD, no load Note 2		0.01	0.3	µA
Conversion current consumption	I_{DD_CONV}	During conversion Cap. Dif. Reg OFF Cap. Ratio Reg OFF Temp Reg ON VDD Mon. Reg OFF Note 3		 580 510 455 455	 850 750 700 700	µA
Average current consumption	I_{DD_AVG}	1 conversion/s, f_{SYS_CLK}=200kHz (SOSC=00) Cap. Dif. Reg OFF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 Note 4		 47.9 24.1 12.2 6.3 3.3	 70.2 35.4 18.0 9.2 4.9	µA
VDD rise time for proper power on reset (POR)	t_{VDD_RISE}	Note 5			1	ms
Internal system clock oscillator frequency Internal system clock oscillator frequency	f_{SYS_CLK}	Normal clock (SOSC=00) Division by 2 (SOSC=01) Division by 4 (SOSC=10) Division by 8 (SOSC=11) TEMPREGEN=0, Note 6	180	200 100 50 25	210	kHz
		Normal clock (SOSC=00) TEMPREGEN=1, Note 6	160	180	200	kHz
Sensor excitation frequency	MCLK	Normal clock (SOSC=00) Division by 2 (SOSC=01) Division by 4 (SOSC=10) Division by 8 (SOSC=11) TEMPREGEN=0	45	50 25 12.5 6.25	52.5	kHz
Capacitance and VDD monitoring conversion time	t_{CONVCV}	Normal clock (SOSC=00) OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 TEMPREGEN=0		 82.6 41.6 21.1 10.9 5.8	 91.7 46.2 23.5 12.1 6.4	ms
Temperature conversion Time	t_{CONVT}	Normal clock (SOSC=00) OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 TEMPREGEN=1		 91.7 46.2 23.5 12.1 6.4	 103.2 52.0 26.4 13.6 7.2	ms

Note 1. Internal regulator must to be enabled only in temperature mode and should be disabled in capacitance and VDD monitoring modes.

Note 2. Leakage current may increase if digital input voltages are not close to VDD (logic level high) or GND (logic level low). Also setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20µA …30µA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.

Note 3. Conversion current consumption values are measured using CS=CR=7.33pF (CS and CR capacitor matrix registers $E3/63_{HEX}$ and $E4/64_{HEX}$ have value 55_{HEX})

Note 4. Average current consumption in other measurement modes can be calculated by scaling these current consumption values with corresponding conversion current ratios. Example: I_{DD_AVG}(Temp Reg ON, OSR=256)=3.3µA*(455µA /580µA)=2.6µA.

Note 5. It is also recommended to reset the device manually either by XCLR pin or using reset register after every power up (VDD rise). In case the VDD rise time is longer than specified here the device has to be kept in a reset during power up by the XCLR pin (XCLR=low). Violating this may risk EEPROM memory integrity. See APPLICATION INFORMATION for examples of external POR circuits.

Note 6. The clock oscillator is factory calibrated. Calibration stored in the Oscillator frequency trim data EEPROM address $(C6/46_{HEX})$.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7V, T_A = -40°C to +85°C, Typ T_A = 27°C, SOSC=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal offset capacitor matrix selection	C_{R_OS}, C_{S_OS} C_{OS_STEP}		0	0.086	22	pF
Changing sensor capacitance range in capacitance difference mode	ΔC_{DIFF}	Normal clock (SOSC=00) Division by 2 (SOSC=01) Division by 4 (SOSC=10) Division by 8 (SOSC=11)	2 2 2 2		20 30 30 30	pF
Maximum allowed sensor capacitance in capacitance difference mode	$C_{S\_MAX\_DIFF}$	Normal clock (SOSC=00) Division by 2 (SOSC=01) Division by 4 (SOSC=10) Division by 8 (SOSC=11) Note 1			20 40 80 160	pF
Changing sensor capacitance range in capacitance ratio mode	ΔC_{RATIO}	Note 2	2		20	pF
Maximum allowed sensor capacitance in capacitance ratio mode	$C_{S\_MAX\_RATIO}$	Note 2			20	pF
Internal temperature sensor	Linearity	Note 3		±0.4		°C
	Gain	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		65056 65038 65002 8116 1012		LSB/°C
		Non-calibrated, note 3	-4.5		+3.5	%
	Offset	Non-calibrated, note 3	-12		+17	°C
RMS temperature resolution		Temp mode, TEMPREGEN=1, OSR=256		0.034		°C
RMS voltage resolution		VDD level monitoring TEMPREGEN=0 OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256 Note 4		 63 72 77 82 99		μV_{RMS}

Note 1. In capacitance difference mode the maximum allowed sensor and reference capacitor values can be extended using lower external oscillator frequency than which is available by SOSC division options; C_{S_MAX}=20pF*200kHz/f_{OSC_EXT}.
Note 2. In capacitance ratio mode also larger capacitances are possible depending on sensor characteristics. Please contact Micro Analog Systems to check sensor suitability.
Note 3. Guaranteed by design. By first order calibration of offset and gain errors an overall temperature accuracy close to the linearity accuracy can be achieved. Further accuracy can be achieved by second order calibration to reduce non-linearity errors. Minimum and maximum values of temperature sensor gain and offset are guaranteed by design.
Note 4. In case of noisy power supply the VDD level monitoring resolution can be further limited by supply noise.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7V, T_A = -40°C to +85°C, Typ T_A = 27°C, SOSC=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RMS capacitance resolution @ ΔC_{LIN}=1.8pF		Difference mode, note 1 TEMPREGEN=0, ΔC_{LIN}=1.8pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 17.2 (15) 16.8 (19) 16.5 (25) 15.8 (39) 15.4 (53)		bit (aF)
RMS capacitance resolution @ ΔC_{LIN}=4pF		Difference mode, note 1 TEMPREGEN=0, ΔC_{LIN}=4pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 17.5 (28) 16.9 (42) 16.1 (69) 15.7 (92) 15.1 (138)		bit (aF)
RMS capacitance resolution @ ΔC_{LIN}=20pF		Difference mode, note 1 TEMPREGEN=0, ΔC_{LIN}=20pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 16.8 (217) 16.2 (337) 15.9 (417) 15.5 (546) 14.6 (1010)		bit (aF)
RMS capacitance resolution @ ΔC_{LIN}=1.8pF		Ratio mode, note 1 TEMPREGEN=0, ΔC_{LIN}=1.8pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 14.3 (115) 14.1 (133) 13.5 (196) 13.0 (276) 12.6 (364)		bit (aF)
RMS capacitance resolution@ ΔCLIN=4pF		Ratio mode, note 1 TEMPREGEN=0, ΔCLIN=4pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 15.2 (130) 14.7 (193) 14.4 (227) 14.0 (296) 13.3 (495)		bit (aF)
RMS capacitance resolution @ ΔCLIN=20pF		Ratio mode, note 1 TEMPREGEN=0, ΔCLIN=20pF OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256		 16.0 (371) 15.7 (468) 15.6 (513) 15.2 (673) 14.6 (1004)		bit (aF)
EEPROM size				256		bit
EEPROM data retention		T_A = +85 °C T_A = +125 °C Note 2	10	24 1		years

Note 1. Resolution in bits is calculated as follows: $C_{N\_BIT}=\log(\Delta C_{FS}/C_N)/\log(2)= \log(CODEFS/CODE_N)/\log(2)$ where ΔC_{FS} and CODEFS are full scale changing capacitance ($\Delta C_{FS}=\Delta C_{LIN}$ /0.8) and code range respectively, C_N and $CODE_N$ are RMS noise in capacitance and code respectively.

Note 2. Data retention values apply when extended EEPROM tests are done. Please contact Micro Analog Systems Oy if the data retention values here need to be guaranteed by comprehensive EEPROM testing.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 2.7V, T_A = -40°C to +85°C, Typ T_A = 27°C, SOSC=00, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Linear output code range values (10%...90% of full scale output code range)	CODELIN	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256	1467187 1466368 1464730 182682 22733		13204685 13197312 13182566 1644134 204595	
Full scale output code range values	CODEFS	OSR=4096 OSR=2048 OSR=1024 OSR=512 OSR=256	0 0 0 0 0		14671872 14663680 14647296 1826816 227328	
VDD sensitivity of capacitance measurement	$VDDSENS_{CAP}$	Difference mode, ΔC_{LIN}=4pF, TEMPREGEN=0, VDD=1.8V ⇒ 3.6V Note 1		+0.03		%FS/V
VDD sensitivity of temperature measurement	$VDDSENS_{TEMP}$	TEMPREGEN=1, VDD=1.9V ⇒ 3.6V Note 1		-0.04		%FS/V

Note 1. VDD sensitivity in %FS/V calculated as follows: VDD_{SENS} =100%*(($CODE @ VDD_{MAX}$) – ($CODE @ VDD_{MIN}$))/CODEFS/(VDD_{MAX} - VDD_{MIN}) where VDD_{MAX}=3.6V, VDD_{MIN}=1.8V in capacitance mode and VDD_{MIN}=1.9V in temperature mode.

Digital inputs

T_A = -40°C to +85°C, VDD = 1.8V to 3.6V, Typ T_A = 27°C, Typ VDD = 2.7 V, R_P = 4.7kΩ (I2C bus pull up) unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		80% VDD		100% VDD	V
Input Low Voltage	V_{IL}		0% VDD		20% VDD	V
Serial Bus Clock Frequency	f_{SCL}	I2C bus SPI bus			400 2	kHz MHz
XCLR Reset Pulse Length	t_{XCLR}	XCLR low pulse	200			ns
Wait time after reset	t_{RESET_WAIT}	Note 1.	20			µs
XCLR Pin Pull Up Current	I_{PULL_UP}	XCLR=0V		-8		µA

Note 1. This is the necessary wait time after reset to allow MAS6510 reading the programmable I2C device address from the EEPROM

Digital outputs

T_A = -40°C to +85°C, VDD = 1.8V to 3.6V, Typ T_A = 27°C, Typ VDD = 2.7 V, R_P = 4.7kΩ (I2C bus pull up) unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage	V_{OH}	I_{Source}=0.6mA	80% VDD		100% VDD	V
Output low voltage	V_{OL}	I_{Sink}=0.6mA	0% VDD		20% VDD	V
Signal rise time (from 10% to 90%)	t_r	EOC pin, C_L=50pF SDA pin, C_B=50pF		14 550		ns
Signal fall time (from 90% to 10%)	t_f	EOC pin, C_L=50pF SDA pin, C_B=50pF		11 11		ns

OPERATING MODES

MAS6510 has two capacitance measurement modes, a temperature measurement mode and a VDD level monitoring mode. In capacitance measurement mode the output is proportional to either capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S. In temperature measurement mode the output is proportional to the absolute temperature. The VDD level monitoring mode allows measuring supply voltage which can be useful especially in battery operated systems.

Measurement mode configuration and start of conversion is done by writing 8-bit configuration data to the Measurement control register (address $E2_{HEX}$). See further details in the Measurement control register chapter.

MAS6510 includes a 256-bit EEPROM memory for storing trim and calibration data on chip. Five bytes (40 bits) of EEPROM are reserved for trim values and programmable I2C device address but the remaining 27 bytes (216 bits) are free for storing sensor calibration and other data.

The stored trim data consists of capacitive front-end offset and gain setting data that are automatically read from EEPROM memory in the beginning of each conversion (in normal operating mode). The programmable I2C device address is read from EEPROM memory only during power on reset or by manual reset using XCLR or the reset register.

The stored calibration data should comprise of calibration and temperature compensation coefficients that can be used to calculate accurate sensor and temperature measurement results from the non-calibrated measurement readings. All calculations need to be done in an external micro controller unit (MCU) which controls the MAS6510.

A calibrated MAS6510 sensor system should be operated as illustrated in figure 2. Connecting VDD triggers power-on-reset (POR) but to make sure the device is reset an additional reset should be given using the XCLR pin or writing any data on the reset register $E0/60_{HEX}$ via the serial bus.

The calibration and compensation coefficients are necessary to be read to the MCU memory only once. From each pair of sensor and temperature measurement readings and using the calibration coefficients the accurate sensor and temperature values can then be calculated in the external MCU.

All communication with MAS6510 is done using either the I2C bus or the SPI bus. Starting an A/D conversion, reading the conversion result and reading and writing data from and to the EEPROM memory are all accomplished via serial bus communication.

In addition to the serial buses the digital interface includes also end-of-conversion (EOC) and master reset (XCLR) pins. See A/D Conversion in the Serial Data Interface (I2C Bus) Control chapter.

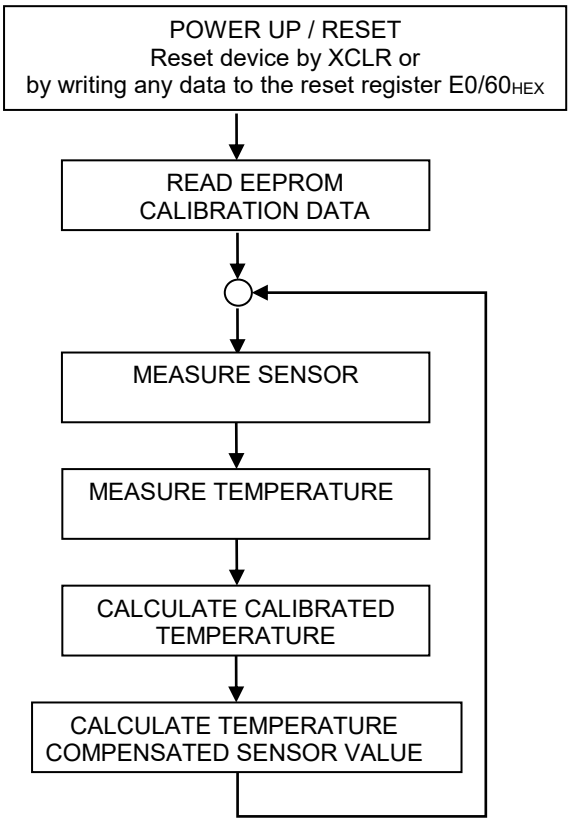


Figure 2. Flow chart for a calibrated MAS6510 sensor system

REGISTER AND EEPROM DATA ADDRESSES

Table 1. Register and EEPROM data addresses

A7	A6	A5	A4	A3	A2	A1	A0	I2C BUS HEX	SPI BUS HEX W=write R=read	Description	Note
A7	1	0	0	0	0	0	X	C0…C1	W: 40…41 R: C0…C1	EEPROM; free for any data	E
A7	1	0	0	0	0	1	0	C2	W: 42 R: C2	Programmable I2C Device Address	E
A7	1	0	0	0	0	1	1	C3	W: 43 R: C3	EEPROM; CS capacitor matrix trim data	E+T
A7	1	0	0	0	1	0	0	C4	W: 44 R: C4	EEPROM; CR capacitor matrix trim data	E+T
A7	1	0	0	0	1	0	1	C5	W: 45 R: C5	EEPROM; Gain trim data	E+T
A7	1	0	0	0	1	1	0	C6	W: 46 R: C6	EEPROM; Oscillator frequency trim data	E+T
A7	1	0	0	0	1	1	1	C7	W: 47 R: C7	EEPROM; free for any data	E
A7	1	0	0	1	X	X	X	C8…CF	W: 48…4F R: C8…CF	EEPROM; free for any data	E
A7	1	0	1	X	X	X	X	D0…DF	W: 50…5F R: D0…DF	EEPROM; free for any data	E
A7	1	1	0	0	0	0	0	E0	W: 60 R: E0	Reset register; no data, only addressed for reset	R
A7	1	1	0	0	0	0	1	E1	W: 61 R: E1	Test register	R
A7	1	1	0	0	0	1	0	E2	W: 62 R: E2	Measurement control register	R
A7	1	1	0	0	0	1	1	E3	W: 63 R: E3	CS capacitor matrix register	R+T
A7	1	1	0	0	1	0	0	E4	W: 64 R: E4	CR capacitor matrix register	R+T
A7	1	1	0	0	1	0	1	E5	W: 65 R: E5	Gain register	R+T
A7	1	1	0	0	1	1	0	E6	W: 66 R: E6	Oscillator frequency control register	R+T
A7	1	1	0	1	0	0	0	E8	W: 68 R: E8	EEPROM data input register	R
A7	1	1	0	1	0	0	1	E9	W: 69 R: E9	EEPROM write enable register	R
A7	1	1	0	1	0	1	0	EA	W: 6A R: EA	1st (MSB) byte of the conversion result	R
A7	1	1	0	1	0	1	1	EB	W: 6B R: EB	2nd (Middle) byte of the conversion result	R
A7	1	1	0	1	1	0	0	EC	W: 6C R: EC	3rd (LSB) byte of the conversion result	R
A7	1	1	0	1	1	0	1	ED	W: 6D R: ED	Status register for EEPROM	R
A7	1	1	0	1	1	1	0	EE	W: 6E R: EE	Trimming control register	R

X = Don't care, E = EEPROM, R= Register, T = Trim data

Note: When using the SPI serial interface the register address bit A7 is also used for selecting write (A7= 0) or read (A7=1) operation. For the I2C interface address bit A7 = 1.
Note: The programmable I2C device address register $C2_{HEX}$ has been factory programmed to value EC $_{HEX}$ (%11101100) which is the same as the hard wired device address of MAS6510. When unique device address is needed it can be programmed to this register.

REGISTER AND EEPROM DATA ADDRESSES

MAS6510 includes a 32 bytes (256 bits) EEPROM data memory and fourteen registers. Five bytes (40 bits) of EEPROM are reserved for trim values and programmable I2C device address but the remaining 27 bytes (216 bits) are free for storing sensor calibration and other data. See table 1 on the previous page for register and EEPROM data addresses.

In the SPI serial bus the address bit A7 selects between write (A7=0) and read (A7=1) operation. In the I2C serial bus A7 is always high (A7=1) and selection between write and read operation is done with the LSB bit of the I2C device address. See table 11 in chapter SERIAL DATA INTERFACE CONTROL. The MAS6510 has both hard wired and programmable I2C device addresses. The programmable device address is factory programmed to value EC $_{HEX}$ (%11101100) which is the same as the hard wired device address of MAS6510. When unique device address is needed it can be programmed to the Programmable I2C Device Address register (C2$_{HEX}$). The MAS6510 will respond to both hard wired and programmed I2C device addresses.

MAS6510 has four trim registers: CS capacitor matrix register (E3/63$_{HEX}$), CR capacitor matrix register (E4/64$_{HEX}$), Gain register (E5/65$_{HEX}$) and Oscillator frequency register (E6/66$_{HEX}$). These are marked with “R+T” in table 1. Each of these registers has a corresponding EEPROM byte where trim values can be permanently stored. These are marked with “E+T” in table 1. Trim values are automatically read from EEPROM in the beginning of each conversion when this feature is enabled in the trimming control register (EE/6E$_{HEX}$). When disabled it is possible to test different trim data in the trim registers before final trimming values are found and stored in the EEPROM.

Reset register (E0/60$_{HEX}$) does not contain any data. Any dummy data written to this register forces a reset. A reset initializes all control registers (addresses E1$_{HEX}$…EE$_{HEX}$) to a zero value.

Test register (E1/61$_{HEX}$) is mainly used for testing and trimming purposes. See table 2 in chapter TEST REGISTER. If an external clock signal is used the test register is needed for selecting the external clock signal.

The Measurement control register (E2/62$_{HEX}$) is used for configuring and starting an A/D conversion.

The CS (E3/63$_{HEX}$) and the CR (E4/64$_{HEX}$) capacitor matrix registers select internal capacitors which are connected from the CS and the CR pins respectively to the CC pin. Both capacitor values can be chosen independently between 0pF and 22pF in 86fF steps.

The Gain register (E5/65$_{HEX}$) controls the gain of the CDC front-end. Together with the CS and CR values the gain determines the input capacitance conversion range.

The Oscillator frequency control register (E6/66$_{HEX}$) is used only during internal clock oscillator trimming. During trimming there is searched register value which gives closest to the nominal 200 kHz oscillator frequency. However the internal clock oscillator frequency is trimmed by MAS during wafer level testing and the trimming value is stored into the Oscillator frequency trim data EEPROM address (C6/46$_{HEX}$). Thus there is no need to adjust the factory stored clock oscillator trimming value. In normal operation the trim value is automatically read from the EEPROM memory in the beginning of each conversion.

EEPROM write enable register (E9/69$_{HEX}$) is used for enabling EEPROM write since by default the EEPROM is write protected.

The 24-bit A/D conversion result (capacitance or temperature) is stored into three registers EA$_{HEX}$ (MSB, most significant byte), EB$_{HEX}$ (ISB, intermediate significant byte), EC$_{HEX}$ (LSB, least significant byte).

The EEPROM status register (ED/6D$_{HEX}$) reflects the EEPROM error correction status. This register can be used to verify that the EEPROM operation has finished without errors.

The Trimming control register (EE/6E$_{HEX}$) defines whether the trim data in the EEPROM or in the registers are used during operation. The default setting is that all trim data is automatically read from the EEPROM memory in the beginning of each conversion. See the Trimming control register description for details.

RESET REGISTER (E0/60HEX)

This register is used to reset all control registers (addresses $E1_H$…EE_H) to a zero value. There are no data bits in this register. However it is necessary to write dummy data to this register to make a reset.

The reset will take place immediately after any data has been written to the address $E0/60_{HEX}$ via the I2C or SPI interface.

TEST REGISTER (E1/61HEX)

In normal operation the Test register value is 00_{HEX} and the internal clock oscillator frequency 200 kHz is used for all the measurements.

FOSC can be used to force the internal oscillator to be on all the time. This is for internal oscillator trimming purpose only. Normally (FOSC=0) the internal oscillator is turned on only during the measurements to save power and the OSC pin output is at logic low. To get the internal 200 kHz clock signal out from OSC pin it is necessary to set FOSC=1.

The SEL_EXTCLK bit selects between internal clock oscillator (OSC pin as digital output) and external clock signal (OSC pin as digital input). External clock selection may come necessary if the sensor capacitance is too high to be used with the internal 200 kHz or divided clock frequency options (see SOSC bits in table 2). The maximum external clock frequency depends on maximum sensor capacitance; f_{EXT}=200kHz*20pF/C_{S_MAX}. Note that if SEL_EXTCLK=1 is selected the internal oscillator is disabled and OSC pin acts as digital input despite of FOSC selection.

The STEST bits are used for connecting different internal signals to the TEST1 and TEST2 pins. In STEST=101 test setup TEST1 and TEST2 operate as positive and negative voltage inputs respectively which are connected to the differential input of the ΔΣ-ADC.

By setting the SOSC bits it is possible to optionally divide the internal system clock frequency by 2, 4 or 8. The undivided 200 kHz system clock frequency allows measuring capacitances up to around 20pF but with the maximum division option 8 capacitances up to 160pF. However note that only sensor base capacitance scales up this much by clock frequency but the maximum changing capacitance range is smaller (see ELECTRICAL CHARACTERISTICS tables).

Note that the frequency division selection SOSC does not apply to OSC pin clock signals. The internal 200 kHz clock signal from OSC pin and the external clock signal applied to OSC pin are not affected by the SOSC divider options.

Table 2. MAS6510 test register (*$E1/61_{HEX}$*) description

Bit Number	Bit Name	Description	Value	Function
7	-	Not used	X	-
6	FOSC	Forces the oscillator on without conversion	0 1	OSC is on only during conversion OSC is forced on
5	SEL_EXTCLK	Selects external clock	0 1	Internal clock, OSC output (default) An external clock (OSC input) can be connected to OSC and the internal oscillator is disabled
4-2	STEST	TEST1 and TEST2 signal selection	000…100 101 110…111	Reserved for internal testing purpose (TEST1 and TEST2 are outputs) TEST1 and TEST2 as inputs No function
1-0	SOSC	Select system clock frequency	00 01 10 11	f_{SYS_CLK} = 200 kHz f_{SYS_CLK} = 100 kHz (div by 2) f_{SYS_CLK} = 50 kHz (div by 4) f_{SYS_CLK} = 25 kHz (div by 8)

X = Don't care

MEASUREMENT CONTROL REGISTER (E2/62HEX)

This register is used to configure and initiate a measurement. See table 3 below. A new conversion is started simply by writing 8-bit configuration data having SCO=1 to the measurement control register (E2/62HEX).

Table 3. Measurement control register (E2/62HEX) description

Bit Number	Bit Name	Description	Value	Function
7-5	OSRS	Over Sampling Ratio (OSR) Selection	000 001 010 011 100	OSR = 256 OSR = 512 OSR = 1024 OSR = 2048 OSR = 4096
4	TEMPREGEN	Temperature Mode Regulator Enable	0 1	Voltage regulator disabled Voltage regulator enabled
3	SCO	Start Conversion	0 1	No conversion Start conversion
2-1	SEL	Capacitive/ VDD Monitoring / Temperature Selection	00 01 10 11	External capacitive sensor VDD level monitoring Internal temperature sensor -
0	XRC	Front end function selector	0 1	Ratio converter Difference converter

The OSRS over sampling ratio selection bits choose between five different OSR values. High OSR value corresponds to high resolution but also longer conversion time. See Electrical characteristics for further details.

The TEMPREGEN bit enables/disables the internal temperature mode voltage regulator. The regulator need to be enabled (TEMPREGEN=1) only in temperature mode and it should be disabled (TEMPREGEN=0) in capacitance and VDD monitoring modes. When enabled the regulator is turned on during conversions and automatically turned off after each conversion to save power. Note also that if in Test register FOSC=1 and if TEMPREGEN=1 the regulator is forced on all the time even when measurement is not running.

The SCO Start conversion bit needs to be set 1 for every new measurement. It is automatically reset to 0 after each measurement.

The SEL sensor selection bits control the front-end multiplexer. It connects either the external capacitive sensor (SEL=00), VDD level monitoring voltage (SEL=01) or the internal temperature sensor (SEL=10) to the $\Delta\Sigma$-converter.

The XRC bit selects between two external capacitive sensor measurement modes. The XRC bit selection does not have any effect on temperature or VDD level monitoring measurements. In Ratio converter mode the output will be proportional to capacitance ratio $(C_S-C_R)/C_S$. In Difference converter mode the output will be proportional to capacitance difference (C_S-C_R).

CS AND CR CAPACITOR MATRIX REGISTERS (E3/63HEX AND E4/64HEX)

There are two internal capacitor matrices that add capacitance in parallel to the sensor capacitor (CS) and the reference capacitor (CR). These offset capacitances are used to adjust the sensor signal to an optimal range. Each capacitor matrix has a selectable capacitance from 0pF up to 22pF in typical 86fF steps. The three sigma process variation of the capacitor matrix capacitance is ±10%.The CS capacitor matrix register (E3/63HEX) has a corresponding EEPROM byte (C3/43HEX) for storing the trim value. Also the CR capacitor matrix register (E4/64HEX) has corresponding EEPROM byte (C4/44HEX) for storing the trim value. After finding suitable CS and CR capacitor matrix register values the trim values can be stored in the corresponding non-volatile EEPROM addresses.

In normal operating mode these trim values are automatically read from the EEPROM during each conversion start. See also table 10 Trimming control Register (EE/6EHEX) for other operating modes.

Table 4. CS capacitor matrix register (E3/63HEX), EEPROM (C3/43HEX)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACS	CDAC control bits	0HEX…FFHEX	CS offset trimming

Table 5. CR capacitor matrix register (E4/64HEX), EEPROM (C4/44HEX)

Bit Number	Bit Name	Description	Value	Function
7-0	OCDACR	CDAC control bits	0HEX…FFHEX	CR offset trimming

GAIN REGISTER (E5/65HEX)

The gain register sets the excitation signal level for the capacitive sensor. The eight bits (GRDAC) can be programmed to values between 0 and 255. Together with the CS and the CR capacitor matrix trim parameters it's used to adjust the sensor signal to an optimal range. The goal is to get a maximum dynamic range and keep the signal within linear input range of the ΔΣ-modulator. This condition is met when the signal minimum and maximum covers the whole linear input range.

The output of MAS6510 has the following relationship to the ΔΣ-modulator output:

$$CODE = Q_{AVE} \cdot CODEFS$$

Q_{AVE} is the average measurement result (from the over sampling) of the ΔΣ-modulator and varies from 0 to 1. The CODEFS is the maximum output code which depends on OSR. See page 5 Full output code range specification in the Electrical characteristics table. The linear signal range of the modulator is from Q_{AVE}=10% to Q_{AVE} =90%.

In case of capacitance difference measurement mode;

$$Q_{AVE} = \frac{1}{2} + \frac{C_S - C_R}{C_{REF}} * \frac{V_S}{2 * V_R}$$

In this mode the gain register value GRDAC sets the V_S level.

V_S= (VDD/1.8V)*(33mV+GRDAC*2.88mV)
V_R = (VDD/1.8V)*144mV
C_S = External sensor + CS matrix capacitance
C_R = External reference + CR capacitance
C_{REF} = 6pF, three sigma variation ±10%
In case of capacitance ratio measurement mode;

$$Q_{AVE} = \left(1 - \frac{C_R}{C_S}\right) * \frac{V_R}{V_S}$$

In this mode the gain register value GRDAC sets the V_S level.

V_S = (VDD/1.8V)*GRDAC*0.52mV
V_R= (VDD/1.8V)*100.8mV
C_S = External sensor + CS matrix capacitance
C_R = External reference + CR capacitance

The gain register (E5/65HEX) has a corresponding EEPROM byte (C5/45HEX). After finding a suitable gain register value it can be stored in the EEPROM memory. In normal operating mode the gain trim value is read automatically from the EEPROM during each conversion start.

Table 6. Gain register (E5/65HEX), EEPROM (C5/45HEX)

Bit Number	Bit Name	Description	Value	Function
7-0	GRDAC	RDAC control bits	0HEX…FFHEX	Gain control by sensor excitation signal level control

OSCILLATOR FREQUENCY CONTROL REGISTER (E6/66$_{HEX}$)

Note that the internal clock oscillator frequency has been factory trimmed and the trim value has been stored in the EEPROM (C6/46$_{HEX}$). It is recommended not to change the factory programmed value!

The oscillator frequency control register (E6/66$_{HEX}$) is for trimming the internal clock oscillator to 200 kHz frequency. This 200 kHz can be measured at the OSC pin. The six LSB bits adjust the oscillator period in 104ns steps. The period increases when the trim value increases. Typically a register value of 28$_{HEX}$ corresponds to the nominal 200 kHz clock oscillator frequency. After finding a suitable trim value it can be stored to the EEPROM (C6/46$_{HEX}$).

Table 7. Oscillator frequency control register (E6/66$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
5-0	OSCF	Oscillator frequency control bits	0$_{HEX}$…3F$_{HEX}$	Oscillator frequency control

EEPROM DATA INPUT REGISTER (E8/68$_{HEX}$)

This register can be ignored by user. It is related to internal EEPROM operations and updated automatically during every EEPROM write operation.

EEPROM WRITE ENABLE REGISTER (E9/69$_{HEX}$)

The EEPROM is normally write protected. To enable write the EEPROM write enable register should be set to %00000100 (04$_{HEX}$). To disable write the register should be set to %00000000 (00$_{HEX}$) which is the register default value after power-on-rest or manual reset by XCLR or reset register. Note: don't use any other EEPROM write enable register values than these two since other register bits are reserved for internal testing purpose only.

Table 8. EEPROM write enable register (E9/69$_{HEX}$)

Bit Number	Bit Name	Description	Value	Function
7-3			00000	Reserved. Keep these bits always 0.
2	EWE	EEPROM write enable	0 1	EEPROM write disabled EEPROM write enabled
1-0			00	Reserved. Keep these bits always 0.

After a power-on-reset and in normal operation the EEPROM write enable register has the default value 00$_{HEX}$.

CONVERSION RESULT REGISTERS (EA…ECHEX)

After measuring capacitance, temperature or supply voltage the 24-bit conversion result is stored into three register addresses EA…ECHEX. The MSB (most significant byte) is at EAHEX, ISB (intermediate significant byte) at EBHEX and LSB (least significant byte) at ECHEX.

EEPROM STATUS REGISTER (ED/6DHEX)

The EEPROM status register (ED/6DHEX) indicates if the stored EEPROM byte is corrupted. The register is updated after each EEPROM data byte read command. See table 9 below. The ERROR bit tells whether a data error has been detected or not.

The DED bit tells whether two or more bit errors have been detected. The EEPROM can correct internally only single bit errors i.e. when ERROR=1 and DED=0. The read EEPROM data byte is corrupted if ERROR=DED=1.

Table 9. MAS6510 EEPROM status register (ED/6DHEX). Only bits (7:6) are used.

Bit Number	Bit Name	Description	Value	Function
7	ERROR	EEPROM error detection	0 1	No errors Error detected
6	DED	EEPROM double error detection	0 1	No errors 2 (or more) data errors
5-0			000000	-

TRIMMING CONTROL REGISTER (EE/6EHEX)

The Trimming control register (EE/6EHEX) is used to select between different trimming operating modes. See table 10 showing the functions of the Trimming control register.

After a power-up reset, master reset via XCLR or a software reset via serial bus the Trimming control register (EE/6EHEX) gets the value %00000000 (00HEX). This is the normal operating mode for a trimmed MAS6510 device. In this mode the capacitive front-end trim values to use (CS, CR and Gain) are automatically read from the EEPROM memory in the beginning of each conversion start.

When calibrating a sensor there is an operating mode in which only the factory calibrated internal oscillator (OSC) clock trim data is read from the EEPROM memory. This mode is selected by writing %10101010 (AAHEX) to the Trimming control register. In this mode it is possible to run conversion tests for different front-end trim register values before suitable values are found and programmed to the EEPROM.

There is also a trimming mode in which all trim data including the internal oscillator trim data is taken from the trim registers rather than from the EEPROM. This mode is selected by writing %11111111 (FFHEX) to the Trimming control register.

Table 10. Trimming control Register (EE/6EHEX)

Bit Number	Bit Name	Description	Value	Function
7-0	REGEE<7:0>	EEPROM control bits	00000000 10101010 11111111 OTHER	All trim data from EEPROM (normal operating mode) Only OSC from EEPROM All trim data from registers All trim data from EEPROM

EEPROM WRITE PROCEDURE

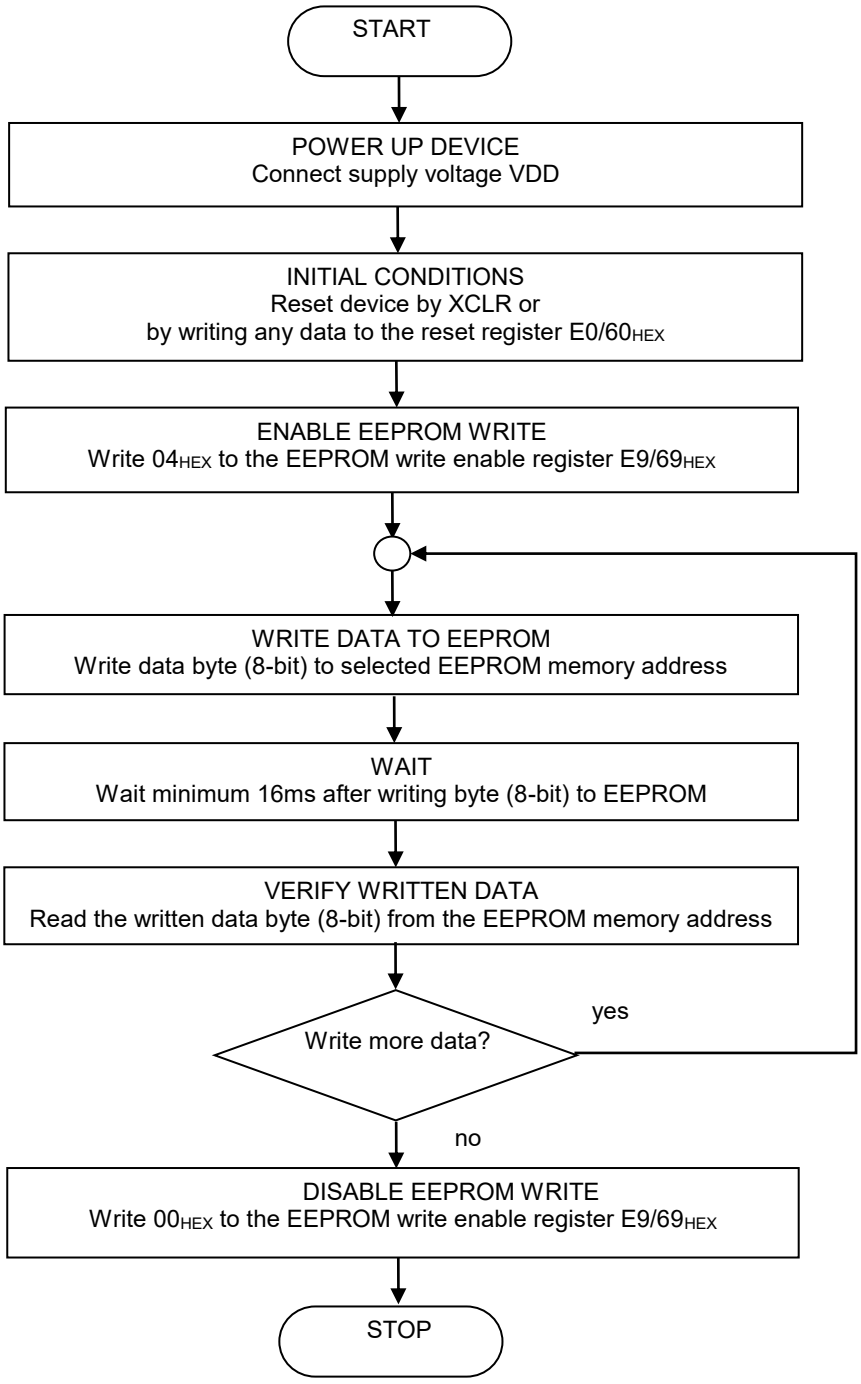


Figure 3. Flow chart for MAS6510 EEPROM write

Important note: Before EEPROM programming make sure that in the Test register (E1/61$_{HEX}$) the SOSC=00 is selected. That selects 200 kHz system clock frequency which is required for the proper EEPROM programming pulses. This condition is guaranteed by making device reset either using the reset register (E0/60$_{HEX}$) or the XCLR pin.
Note: In the “VERIFY WRITTEN DATA” step it could be also additionally checked that the EEPROM status register (ED/6D$_{HEX}$) does not indicate read errors.

EEPROM WRITE PROCEDURE

This chapter gives instructions for writing data to the EEPROM memory.

The MAS6510 24-bit Capacitance-to-Digital Converter (CDC) has a 256 bit (32 bytes) EEPROM memory. 8 bits (1 byte) has been reserved for storing internal clock oscillator trimming data and other 8 bits (1 byte) for the programmable I2C device address. There are also 24 bits (3 bytes) for trimming the capacitive sensor front-end. The remaining 216 bits (27 bytes) are free for storing sensor calibration data and other use.

See figure 3 on previous page showing the EEPROM write procedure.

Make sure in the beginning of the EEPROM write procedure that the MAS6510 initial conditions are met. Connecting VDD triggers power-on-reset (POR) but to make sure the device is reset an additional reset should be given using the XCLR pin or writing any data on the reset register $E0/60_{HEX}$ via the serial bus. The device reset will guarantee that SOSC=00 is selected in the test register ($E1/61_{HEX}$). This selects 200 kHz clock which is required in the EEPROM programming.

EEPROM write is enabled by writing value 04_{HEX} to the EEPROM write enable register ($E9/69_{HEX}$). The default register value after power on is 00_{HEX}.

Next the data can be written to the EEPROM memory one byte (8-bit) at a time. It is necessary to have a delay of minimum 16ms after programming each byte (8-bit). The success of each write can be verified by reading back the data (8-bit) and comparing it to the original byte (8-bit). Additionally it is also possible to check the EEPROM status register ($ED/6D_{HEX}$) value after each read back. The EEPROM status register value should be 00_{HEX} when the read EEPROM data byte is free of errors.

After all data bytes are written the EEPROM memory can be protected from write by writing 00_{HEX} to the EEPROM write enable register ($E9/69_{HEX}$).

See table 1 showing the MAS6510 register and EEPROM data addresses.

SERIAL DATA INTERFACE CONTROL

Serial Interface

MAS6510 can be operated either via 2-wire serial I2C bus or via 4-wire serial SPI bus. Selection between I2C and SPI communication is done by XSPI pin. XSPI=high selects I2C and XSPI=low selects SPI communication.

2-wire serial I2C bus type interface comprises of serial clock input (SCL) and bi-directional serial data (SDA) input/output. I2C bus is used to write configuration data to sensor interface IC and read the measurement result when A/D conversion has been finished. The interface is also used for reading the calibration EEPROM memory.

Note: The 2-wire I2C bus of MAS6510 supports only basic I2C bus communication protocol but not for example 10-bit addressing, arbitration and clock stretching features of the I2C bus specification.

The alternative 4-wire serial SPI bus type interface comprises of serial clock input (SCLK), serial data input (MOSI), serial data output (MISO) and chip select input (XCS).

Digital interface includes also end of conversion (EOC) and master reset (XCLR) pins. Rising edge in the EOC pin indicates that the conversion is ready and the result can be read out through serial interface.

XCLR is used to reset the MAS6510. A reset initializes registers (set to value 00_{HEX}), counters and the serial communication bus. Alternatively device can be reset via serial bus by writing any data to Reset register (address $E0/60_{HEX}$). The Reset register bits don't have any function. Reading from the reset register is not possible.

After connecting the supply voltage to MAS6510, and before starting operating the device via the serial bus, it is required to reset the device if the supply voltage rise time has been longer than 1ms. However it is recommended to reset the device manually after every power up to guarantee proper register settings after any VDD rise conditions

I2C Bus Communication

In MAS6510 the I2C bus communication is selected by setting XSPI pin high.

The I2C bus standard makes it possible to connect several devices on same bus. The devices are distinguished from each other by unique device addresses. In MAS6510 there is both a hard wired and programmable device address. Both hard wired and programmable addresses can be used to address MAS6510. The MAS6510 hard wired device address is shown in the following table. The LSB bit of the device address defines whether the bus is configured to Read (1) or Write (0) operation.

The programmable device address is located in the EEPROM register $C2_{HEX}$ which has been factory programmed to value EC_{HEX} (%11101100) which is the same as the fixed device address of MAS6510. When unique device address is needed it can be programmed to this register. The programmable I2C device address is read from EEPROM memory only during power on reset or manual reset situations. To guarantee that the programmable address is read from EEPROM the device can be reset manually by using XCLR pin or Reset register ($E0/60_{HEX}$).

Table 11. MAS6510 hard wired I2C bus device address (EC/ED_{HEX})

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	1	0	1	1	0	0/1

I2C Bus Protocol Definitions

Data transfer is initiated with a Start bit (S) when SDA is pulled low while SCL stays high. Then, SDA sets the transferred bit while SCL is low and the data is sampled (received) when SCL rises. When the transfer is complete, a Stop bit (P) is sent by releasing the data line to allow it to be pulled up while SCL is constantly high.

Figure 4 shows the start (S) and stop (P) bits and a data bit. Data must be held stable at the SDA pin when SCL is high. Data at the SDA pin can change value only when SCL is low.

Each SDA line byte transfer must contain 8-bits where the most significant bit (MSB) always comes first. Each byte has to be followed by an acknowledge bit (see further below). The number of bytes transmitted per transfer is unrestricted.

2-WIRE SERIAL DATA INTERFACE (I2C BUS)

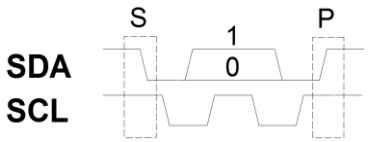


Figure 4. I2C bus protocol definitions

Bus communication includes Acknowledge (A) and not Acknowledge (N) messages. To send an acknowledge the receiver device pulls the SDA low for one SCL clock cycle. For not acknowledge (N) the receiver device leaves the SDA high for one SCL clock cycle in which case the master can then generate either a Stop (P) bit to abort the transfer, or a repeated Start (Sr) bit to start a new transfer.

Abbreviations:
A= Acknowledge by Receiver
N = Not Acknowledge by Receiver
S = Start
Sr = Repeated Start
P = Stop
= from Master (MCU) to Slave (MAS6510)
= from Slave (MAS6510) to Master (MCU)

Conversion Starting – Write Sequence

Conversion is started by writing configuration bits into the Measurement control register (address $E2_{HEX}$). The write sequence is illustrated in Table 12.

Table 12. MAS6510 I2C bus write sequence of Measurement control register

S	AW	A	MC	A	DC	A	P

Abbreviations:
AW = Device Write Address EC_{HEX} (%1110 1100)
AR = Device Read Address ED_{HEX} (%1110 1101)
MC = Meas. control register 62_{HEX} (%0110 0010)
Ax = Conversion Result Registers' Addresses; MSB (x=M, $6A_{HEX}$ %0110 1010), ISB (x=I, $6B_{HEX}$ %0110 1011) or LSB (x=L, $6C_{HEX}$ %0110 1100)
DC = Measurement Control Register Data
Dx = Conversion Result Register Data; MSB (x=M), ISB (x=I) or LSB (x=L)

Each serial bus operation, like write, starts with the start (S) bit (see figure 4). After start (S) the MAS6510 device address with write bit (AW, see table 11) is sent followed by an Acknowledge (A). After this the Measurement control register address (see table 1) is sent and followed by an Acknowledge (A). Next the Measurement control register data (DC, see table 3) is written and followed by an Acknowledge (A). Finally the serial bus operation is ended with stop (P) command (see figure 4). A new A/D conversion starts right after Measurement control register bits containing SCO=1 are received.

A/D Conversion

After power on reset or external reset (XCLR) the EOC output is high. After an A/D conversion is started the EOC output is set low until the conversion is finished and the EOC goes back high, indicating that the conversion is done and data is ready for reading. The EOC is set low only by starting a new conversion. To save power the internal oscillator runs only during conversion.
During an A/D conversion the input signal is sampled continuously leading to an output conversion result that is a weighted average of the samples taken.

2-WIRE SERIAL DATA INTERFACE (I2C BUS)

Conversion Result – Read Sequence

Table 13 presents a general control sequence for a single register data read.

Table 13. MAS6510 I2C bus single register (address Ax) read sequence bits

S	AW	A	Ax	A	Sr	AR	A	Dx	N	P

Table 14 shows the control sequence for reading the 24-bit A/D conversion result from the Conversion result registers. The ISB (DI) and LSB (DL) register data read can follow right after the MSB register data (DM) read since if the read sequence is continued (not ended by a Stop bit P) the register address is automatically incremented to point to the next register.

Table 14. MAS6510 I2C bus MSB (first), MID (second) and LSB (third) A/D conversion result read sequence

S	AW	A	AM	A	Sr	AR	A	DM	A	DI	A	DL	N	P

4-WIRE SERIAL DATA INTERFACE (SPI BUS)

SPI bus communication is selected by setting XSPI pin low.

SPI communication differs from I2C bus in the following way. It requires four wires for bi-directional communication since each line operates in one direction only. Device selection is done by using separate chip select XCS control lines instead of using device address. Each SPI bus device has its own XCS control line and a device is selected by pulling its XCS line low (see figure 5 below). The fourth wire in the SPI bus is the serial clock line, SCLK. Data is transferred at rising edges of the serial clock during which the data line should be stable.

The selection between write or read access is done by register address MSB bit A7 (see table 1 "*Register and EEPROM data addresses*"). In write access bit A7 cleared (0) and in read access it is set (1).

Figure 5 illustrates write access communication. MAS6510 has an auto increment function which means that if there are more than one data byte transferred the additional data bytes are delivered to following register addresses. In write communication the MISO line is high impedance.

In SPI bus communication it is good to note that setting XCS low activates the EEPROM memory regardless of the XSPI setting and the device consumes 20µA …30µA current. To minimize current consumption XCS should be set low only during time periods when the device is used during SPI communication.

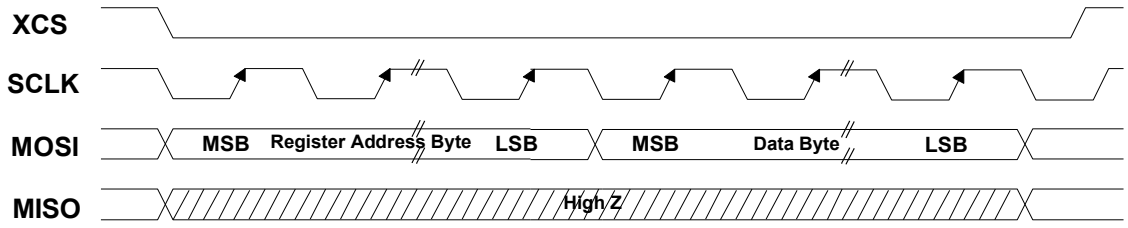


Figure 5. *SPI Protocol – Write Access (register address MSB bit A7=0)*

4-WIRE SERIAL DATA INTERFACE (SPI BUS)

Figure 6 illustrates read access communication. The auto increment function can be utilized also in read access and if there are more than one data byte read the additional data bytes are delivered from following register addresses.

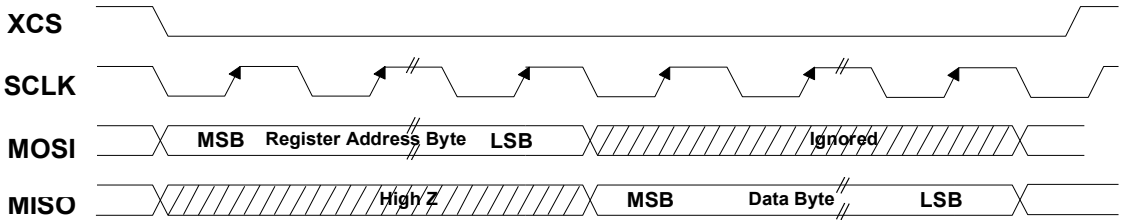


Figure 6. *SPI Protocol – Read Access (register address MSB bit A7=1)*

TRIMMING FOR SENSOR CAPACITANCE

MAS6510 has two different capacitance measurement modes. The output can be proportional either to capacitance difference (C_S-C_R) or to capacitance ratio (C_S-C_R)/C_S.

For trimming it is necessary to know the sensor capacitance C_S range $C_{S\ MIN}$…$C_{S\ MAX}$. For optimal utilization of the MAS6510 input range the trimming is based on selecting the minimum linear range capacitance same as $C_{S\ MIN}$ and maximum linear range capacitance same as $C_{S\ MAX}$. At the linear range minimum and maximum limits the average of the ΔΣ-modulator output is 10% and 90% respectively. In the following trimming equations we denote these by

D_{MIN} = 0.1
D_{MAX} = 0.9

In the capacitance measurement the internal regulator should be disabled (TEMPREGEN=0) and the external capacitive sensor selected (SEL=00).

MAS6510 in capacitance difference mode

The reference capacitor value C_R is calculated from

$C_R = [C_{S\ MIN}*(D_{MAX}-0.5)-C_{S\ MAX}*(D_{MIN}-0.5)] / (D_{MAX}-D_{MIN})$

If an external C_R is used, it is connected between pins CR and CC. If an internal C_R is used, the trim code for C_R is calculated from

$REG_{E4HEX} = (C_R/C_{R\ MAX})*255$

where $C_{R\ MAX}$ is nominally 22pF, but subject to ±10 % (±3 sigma) process variation.

The reference voltage, V_S, can be calculated using the following equation:

$V_S = [144mV*(D_{MAX}-D_{MIN})*2*C_{REF}] / (C_{S\ MAX}-C_{S\ MIN})$

where C_{REF} is nominally 6 pF, but also has ±10 % variation.

The gain register trim value is calculated from

$REG_{E5HEX} = [(V_S-33\ mV) / 734mV]*255$

REG_{E4HEX} and REG_{E5HEX} are 8-bit values, so they range from 0 to 255. When their values are found, the same values can be written to corresponding EEPROM addresses $C4_{HEX}$ and $C5_{HEX}$. However, with SPI bus, the address MSB in write operation is 0, so the addresses are actually 44_{HEX} and 45_{HEX}.

Example: Single capacitance sensor

$C_{S\ MIN}$=8pF
$C_{S\ MAX}$=12pF
$C_R = [8pF*(0.9-0.5)-12pF*(0.1-0.5)]/(0.9-0.1) = 10pF$
$REG_{E4HEX} = (10pF/22pF)*255 = 115.9 \sim 116$
$V_S = [144mV*(0.9-0.1)*2*6pF] / (12pF-8pF) = 345.6mV$
$REG_{E5HEX} = [(345.6-33\ mV) / 734mV]*255 = 108.6 \sim 109$
REG_{E3HEX} = 0 (no internal C_S capacitor matrix used)

TRIMMING FOR SENSOR CAPACITANCE

MAS6510 in capacitance ratio mode

The reference capacitor C_R is calculated from

$C_R = [C_{S\,MIN}*C_{S\,MAX}*(D_{MAX}-D_{MIN})] / (C_{S\,MAX}*D_{MAX}-C_{S\,MIN}*D_{MIN})$

If an external C_R is used, it is connected between pins CR and CC. If an internal C_R is used, the trim code for C_R is calculated from

$REG_{E4HEX} = (C_R/C_{R\,MAX})*255$

where $C_{R\,MAX}$ is nominally 22pF, but subject to ±10 % (±3 sigma) process variation.

The reference voltage, V_S, can be calculated using the following equation:

$V_S = 100.8mV * (C_{S\,MAX}-C_{S\,MIN}) / (C_{S\,MAX}*D_{MAX}-C_{S\,MIN}*D_{MIN})$

The gain register trim value is calculated from

$REG_{E5HEX} = (V_S / 133.3mV)*255$

REG_{E4HEX} and REG_{E5HEX} are 8-bit values, so they range from 0 to 255. When their values are found, the same values can be written to corresponding EEPROM addresses $C4_{HEX}$ and $C5_{HEX}$. However, with SPI bus, the address MSB in write operation is 0, so the addresses are actually 44_{HEX} and 45_{HEX}.

Example: Single capacitance sensor

$C_{S\,MIN}$=8pF
$C_{S\,MAX}$=12pF
$C_R = [8pF*12pF*(0.9-0.1)] / (12pF*0.9-8pF*0.1) = 7.68pF$
$REG_{E4HEX} = (7.68pF/22pF)*255 = 89.0 \sim 89$
$V_S = 100.8mV*)/(12pF-8pF)/(12pF*0.9-8pF*0.1)=40.32mV$
$REG_{E5HEX} = (40.32mV/133.3mV)*255 = 77.1 \sim 77$
REG_{E3HEX} = 0 (no internal C_S capacitor matrix used)

TEMPERATURE MODE

The MAS6510 has an internal temperature sensor for temperature measurement. The temperature sensor output is proportional to absolute temperature (PTAT). The temperature information is needed for temperature indication and temperature compensation.

The temperature measurement is started by writing configuration data to the measurement control register (E2/62$_{HEX}$). In the temperature measurement the internal regulator has to be enabled (TEMPREGEN=1) and the internal temperature sensor selected (SEL=10). The ratio and difference converter bit (XRC) selection does not have any influence on the result. Typically already the smallest over sampling ratio (OSR) selection 256 offers sufficient resolution for the temperature measurement.

The internal temperature sensor has offset and gain variation but small non-linearity (see Electrical Characteristics table). Depending on temperature measurement accuracy requirement the offset, the gain and the non-linearity all can be compensated by external calculations. In low precision the offset and gain calibration is sufficient but in high precision the second order non-linearity calibration can be included.

Linear temperature sensor model

The linear temperature measurement model for output code is following.

$$CODE = CODEFS \cdot \left(a + b \cdot \left(T - T_{REF}\right)\right)$$

The OSR selects full scale output code range value CODEFS. See Electrical Characteristics for CODEFS$_{DIFF}$ at different OSR values. If the temperature T is presented in °C and referenced to T$_{REF}$=0°C then the typical linearized temperature sensor model parameter values a and b are as follows.

a=0.38944
b=4.4329e-3

However it should be noted that the sensor has significant offset (parameter a) variation and also the gain (parameter b) has some variation and that the above values represent only typical values. The non-linearity temperature error after offset and gain calibration (best fit line) is typically <±0.5°C in the temperature range -40°C…+85°C.

2nd order temperature sensor model

For higher precision the 2nd order temperature measurement model for output code is following

$$CODE = CODEFS \cdot \left(a + b \cdot \left(T - T_{REF}\right) + c \cdot \left(T - T_{REF}\right)^2\right)$$

If the temperature T is presented in °C and referenced to T$_{REF}$=0°C then the typical 2nd order temperature sensor model parameter values a, b and c are as follows.

a=0.38826
b=4.3967e-3
c=8.1098e-7

Above sensor model parameters are typical values which are subject to variations. The temperature error after offset, gain and 2nd order non-linearity calibration is typically <±0.1°C in the temperature range -40°C…+85°C.

VDD LEVEL MONITORING MODE

The MAS6510 has VDD level monitoring feature to measure supply voltage level which is useful especially in battery operated systems. In systems in which VDD can vary the VDD level monitoring could be also used to compensate VDD dependency.

The VDD level monitoring measurement is started by writing configuration data to the measurement control register (E2/62$_{HEX}$). In the VDD level monitoring mode the regulator has to be disabled (TEMPREGEN=0) and VDD level monitoring selected (SEL=01). The ratio and difference converter bit (XRC) selection does not have any influence on the result.

Typically the smallest over sampling ratio (OSR) selection 256 offers sufficient resolution for the VDD level monitoring.

VDD level monitoring model

The VDD level monitoring model for output code is following.

$$CODE = CODEFS \cdot \left(a - \frac{b}{VDD} \right)$$

The output has inverse relationship to supply voltage VDD. The OSR selects full scale output code range value CODEFS. See Electrical Characteristics for CODEFS at different OSR values.

The typical VDD level monitoring model parameter values a and b are as follows.
a=1.6375
b=2.6942
Note that these parameter values are subject to about two percent variations.

The supply voltage VDD can be solved from the output result as follows.

$$VDD = \frac{b}{a - \frac{CODE}{CODEFS}}$$

Figure 7 presents typical output code as function of supply voltage at OSR=256 (CODEFS=227328).
Figure 8 present supply voltage as function of output code at OSR=256 (CODEFS=227328).

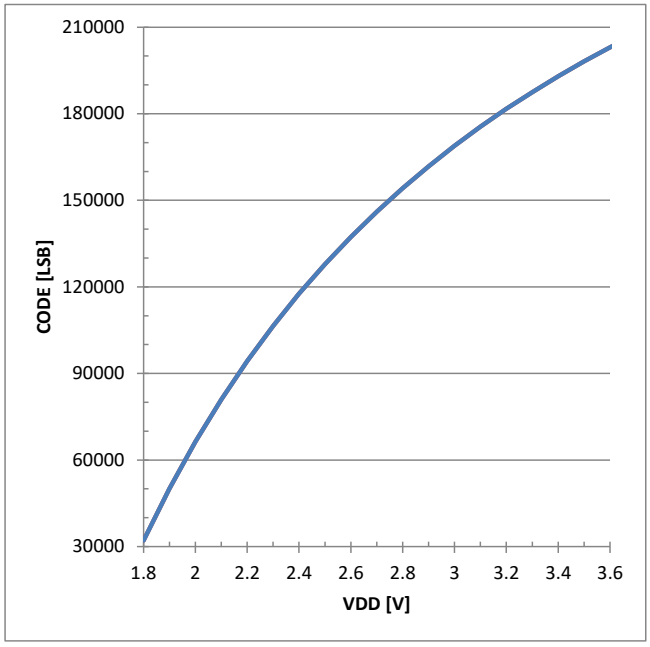


Figure 7. CODE(VDD) at VDD level monitoring

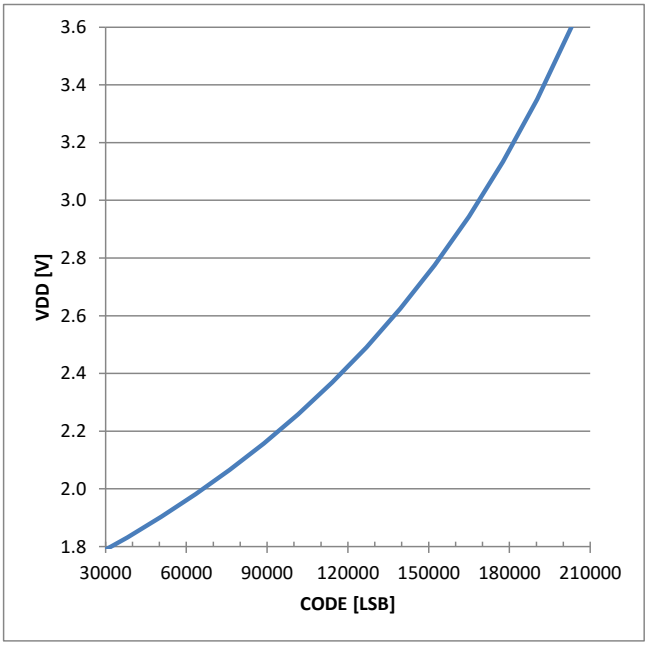
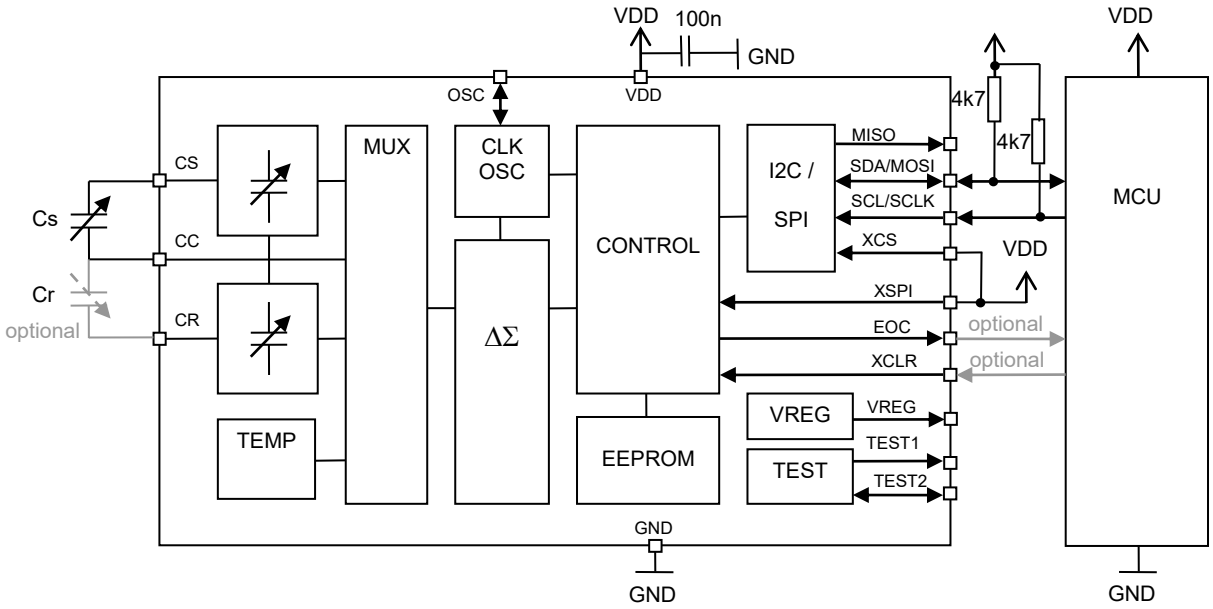


Figure 8. VDD(CODE) at VDD level monitoring

APPLICATION INFORMATION

VDD rise time < 1ms



NOTE: It is recommended to use the XCLR reset feature to solve unexpected error state conditions. In case VDD rise time can exceed 1ms the device has to be kept in a reset during power up by using the XCLR pin. Violating this may risk EEPROM integrity. If not used the XCLR pin can be left unconnected since it has internal pull up to VDD.

Figure 9. MAS6510 configured for I2C bus communication

Note: MAS6510 has an effective ESD clamp protection structure that can be triggered if the VDD rises too fast. For this reason it's recommended to use a supply decoupling capacitor having a value of 100nF or higher to slow down the VDD rise time.

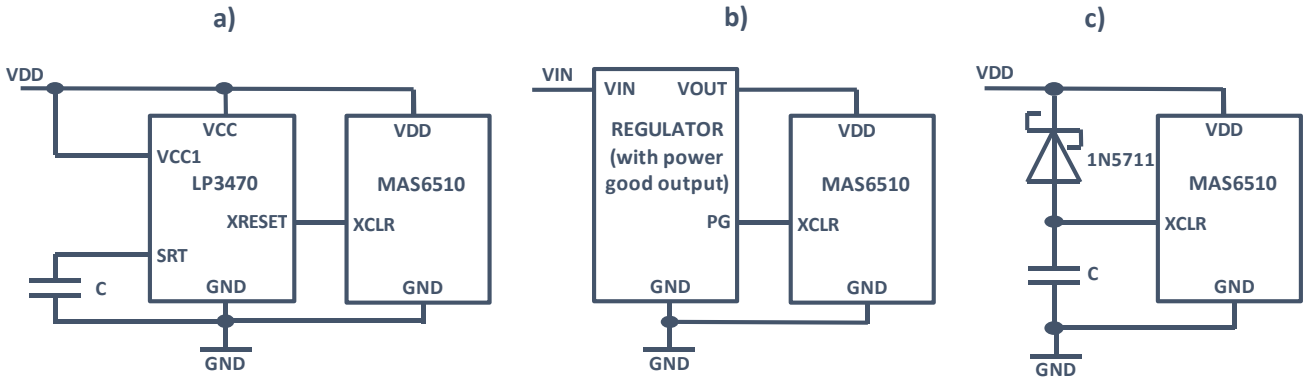
Note: The voltage regulator output VREG does not require external capacitor as shown in figure 9. However if an output capacitor is wanted to be used for extra filtering the capacitor value should not be higher than 6.8nF.

Figure 9 presents MAS6510 application circuit using I2C bus and when VDD rise time is guaranteed to be always below internal POR circuit delay of 1ms. In case the VDD rise time can exceed 1ms see the next page application information.

APPLICATION INFORMATION

VDD rise time > 1ms

If the VDD rise time can exeed 1ms it is necessary to keep the MAS6510 in reset during power up using the XCLR reset pin. Violating this may risk EEPROM memory integrity. Figures 10 a-c present examples of external POR circuits providing reset via the XCLR pin in case the VDD rise time can exceed 1ms.



Figures 10 a, b, c. External XCLR reset circuit examples for VDD rise time >1ms

The XCLR pin has internal pull up with 8µA current which makes the pull up resistor unnecessary. In the figure 10c the external POR circuit delay can be calculated as follows.

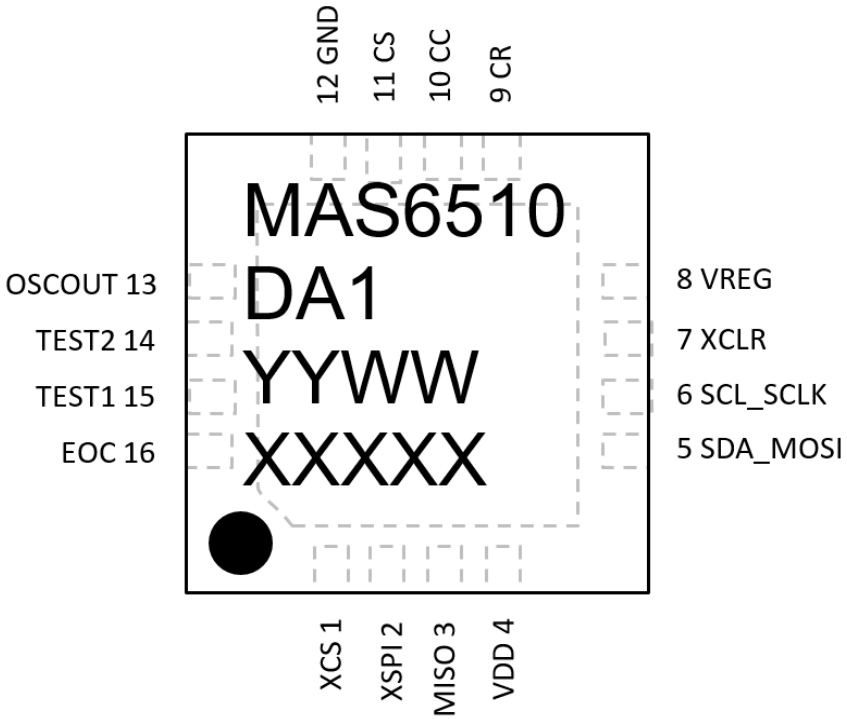
$$t_{POR} = \frac{C}{8\mu A} \cdot VDD$$

The POR delay should be made larger than the maximum VDD rise time. For example if the longest possible VDD rise time is 50ms and VDD=2.7V then we could choose capacitor value which gives at least 100ms POR delay; C=8µA*t_{POR}/VDD=8µA*100ms/2.7V=296nF which is rounded up to 330nF.

Resolution Improvement – Averaging

An averaging technique can be used to remove conversion errors caused by noise and thus improve measurement resolution. By doing several A/D conversions and calculating the average result it's possible to average out noise. Theoretically the noise is reduced by a factor $\sqrt{N}$ where N is the number of averaged samples. A/D converter nonlinearities cannot be removed by averaging.

MAS6510 IN QFN-16 4x4x0.75 PACKAGE



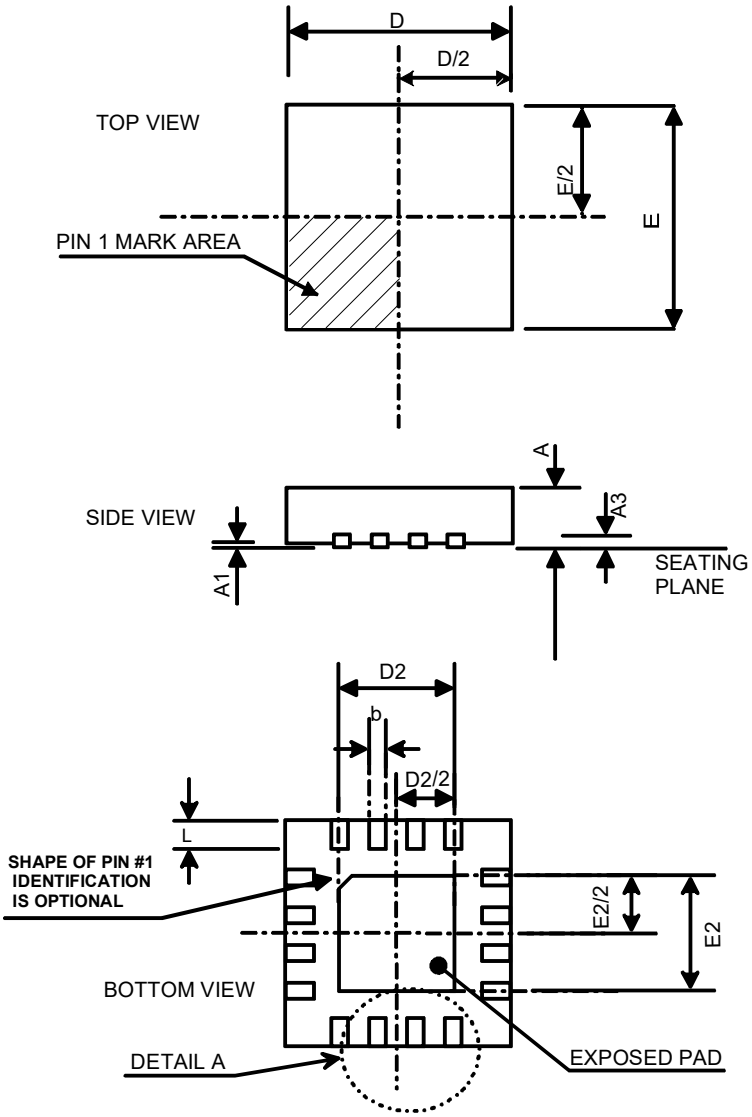
Top Marking Information:
MAS6510 = Product Number,
DA1 = Version Number
YYWW = Year Week
XXXXX = Lot Number

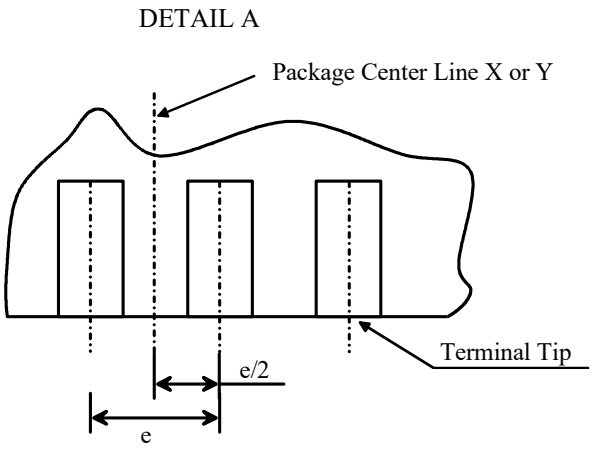
QFN-16 4x4x0.75 PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
XCS	1	DI	Chip Select (SPI)	
XSPI	2	DI	SPI / I2C Bus Selection SPI: XSPI=low I2C: XSPI=high	
MISO	3	DO	Master Input Slave Output (SPI)	
VDD	4	P	Power Supply Voltage	
SDA_MOSI	5	DI/O	Serial Bus Data (I2C) Master Output Salve Input (SPI)	
SCL_SLCK	6	DI	Serial Bus Clock (I2C / SPI)	
XCLR	7	DI	Master Reset	1
VREG	8	AO	Voltage Regulator Output 1.8V	
CR	9	AO	Reference Capacitance Pin	
CC	10	AI	Common Capacitance Pin	
CS	11	AO	Sensing Capacitance Pin	
GND	12	G	Power Supply Ground	
OSC	13	DI/DO	Oscillator Input / Output	
TEST2	14	AI/O	Test pin 2	
TEST1	15	DO	Test pin 1	
EOC	16	DO	End of Conversion	

P = Power, G = Ground, DO = Digital Output, , DI = Digital Input, AO = Analog Output, AI = Analog Input
Note 1: The XCLR pin has internal pull up to VDD. If not used the XCLR pin can be left unconnected.
Note: The exposed pad of the QFN package should be connected to the GND.

PACKAGE (QFN-16 4X4x0.75) OUTLINE





Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3		0.203 REF		mm
b	0.250	---	0.350	mm
D	3.950	4.000	4.050	mm
D2 (Exposed.pad)	2.700	---	2.900	mm
E	3.950	4.000	4.050	mm
E2 (Exposed.pad)	2.700	---	2.900	mm
e		0.650 BSC		mm
L	0.350	---	0.450	mm

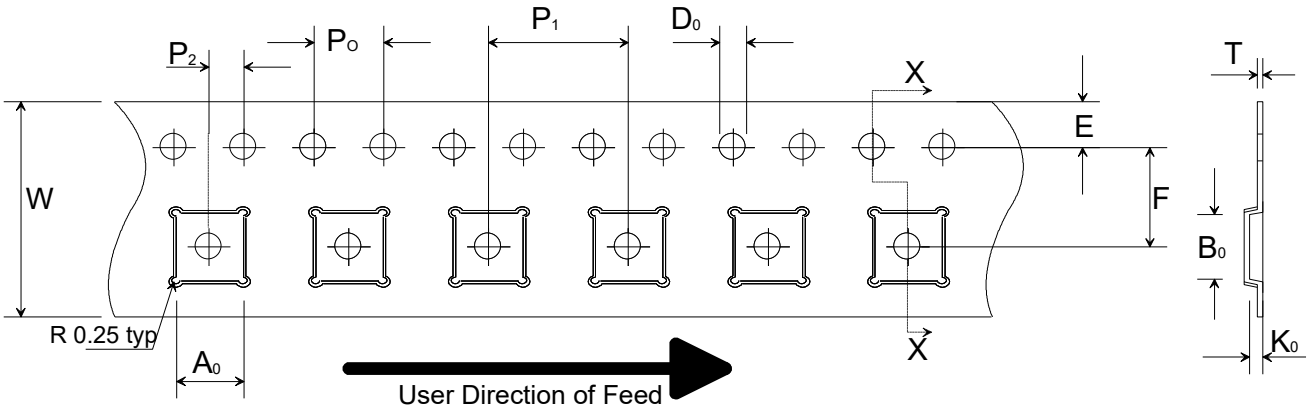
Dimensions do not include mold or interlead flash, protrusions or gate burrs.

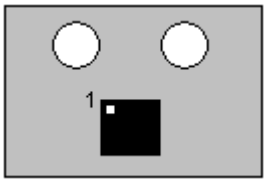
SOLDERING INFORMATION

◆ **For Lead-Free / Green QFN 4mm x 4mm**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS



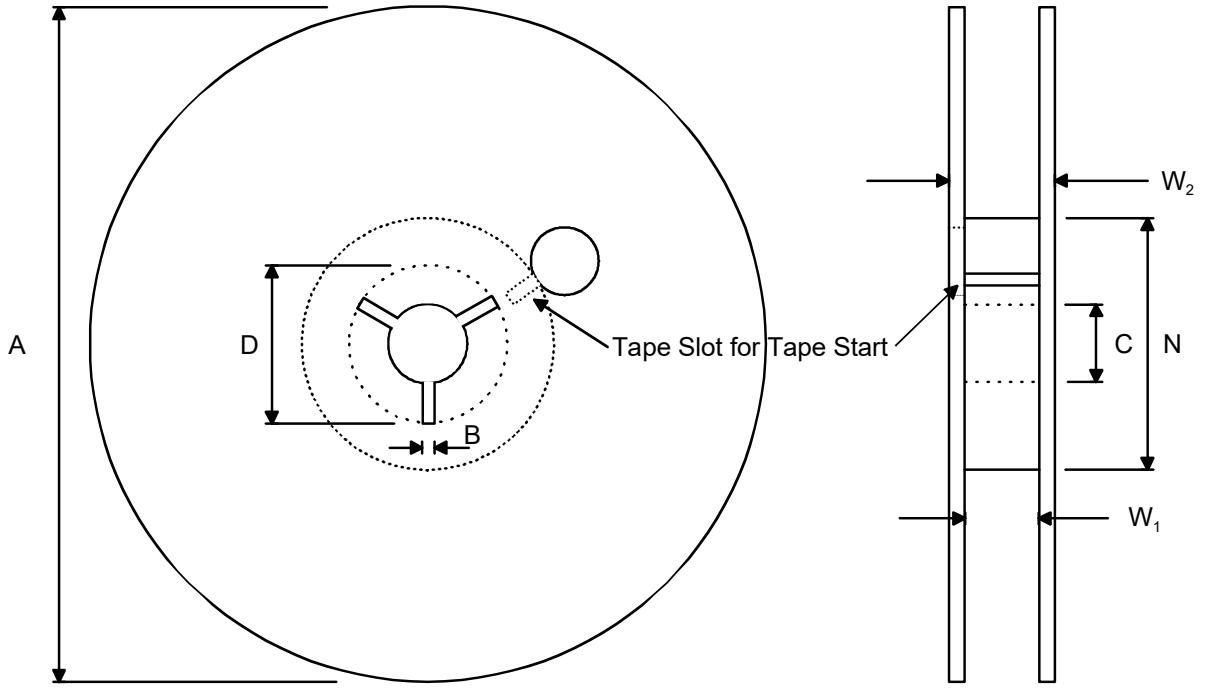


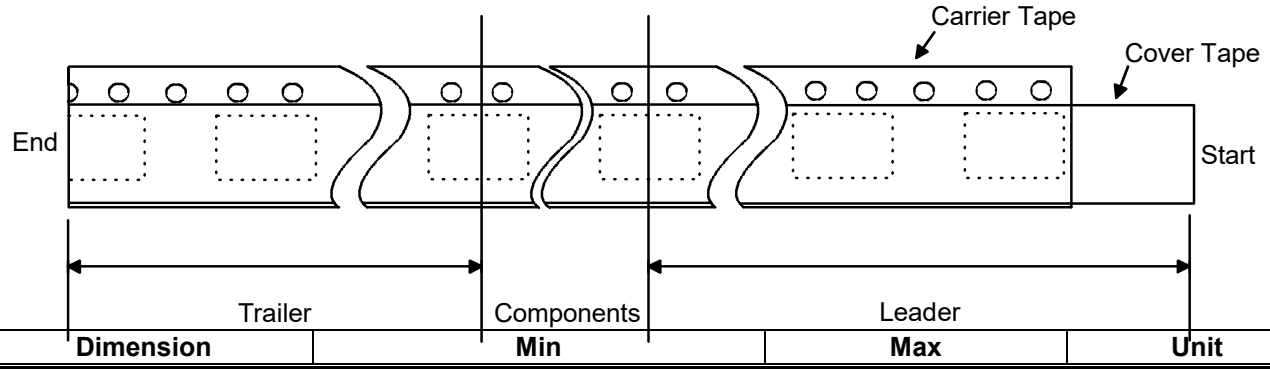
Orientation on tape

Dimension	Min/Max	Unit
A_o	4.30 ±0.10	mm
B_o	4.30 ±0.10	mm
D_o	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
K_o	1.10 ±0.10	mm
P_o	4.0	mm
P_1	8.0 ±0.10	mm
P_2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

All dimensions in millimeters

REEL SPECIFICATIONS





Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	100		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Description
MAS6510DA1WAD00	Capacitive Sensor Signal Interface IC	EWS-tested wafer, thickness 370 µm
MAS6510DA1WAB05	Capacitive Sensor Signal Interface IC	Dies on waffle pack, thickness 180 µm
MAS6510DA1Q1706	Capacitive Sensor Signal Interface IC	QFN-16 4x4x0.75 Package, Pb-free, RoHS compliant, Tape & Reel, 1000 / 3000 pcs components on reel

Contact Micro Analog Systems Oy for other wafer and die thickness options.

LOCAL DISTRIBUTOR

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