

# MAS9081

- **Dual Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

## DESCRIPTION

The MAS9081 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiving. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain

control) can be used to switch AGC on or off if necessary. MAS9081 supports dual band operation by switching between two crystal filters and an additional antenna tuning capacitor.

MAS9081 has differential input and different internal compensation capacitor options for compensating shunt capacitances of different crystals (See ordering information on page 12).

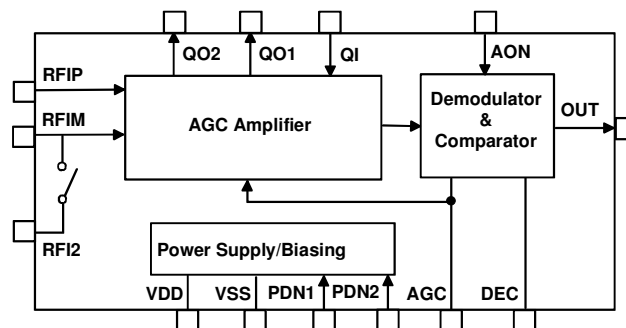
## FEATURES

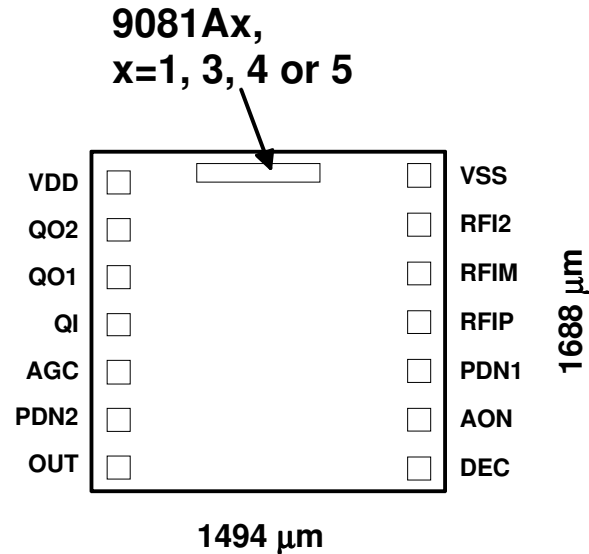
- Dual Band Receiver IC
- Highly Sensitive AM Receiver,  $0.4 \mu\text{V}_{\text{RMS}}$  typ.
- Wide Supply Voltage Range from 1.1 V to 5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

## APPLICATIONS

- Dual Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

## BLOCK DIAGRAM



**MAS9081 PAD LAYOUT**


DIE size = 1.49 x 1.69 mm; PAD size = 80 x 80 μm

**Note:** Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

**Note:** Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	174 μm	1452 μm	
Quartz Filter Output for Crystal 2	QO2	174 μm	1247 μm	
Quartz Filter Output for Crystal 1	QO1	174 μm	1043 μm	
Quartz Filter Input for Crystals	QI	174 μm	839 μm	
AGC Capacitor	AGC	174 μm	633 μm	
Power Down/Frequency Selection Input 2	PDN2	174 μm	430 μm	3
Receiver Output	OUT	175 μm	224 μm	1
Demodulator Capacitor	DEC	1318 μm	240 μm	
AGC On Control	AON	1318 μm	444 μm	2
Power Down/Frequency Selection Input 1	PDN1	1318 μm	648 μm	3
Positive Receiver Input	RFIP	1318 μm	853 μm	4
Negative Receiver Input	RFIM	1318 μm	1057 μm	4
Receiver Input 2 (for Antenna Capacitor 2)	RFI2	1318 μm	1262 μm	
Power Supply Ground	VSS	1318 μm	1466 μm	

**Notes:**

- 1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- 2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- 3) PDN1 = VDD and PDN2 = VDD means receiver off
  - Fast start-up is triggered when the receiver is after power down controlled to power up
- 4) Receiver inputs RFIP and RFIM have both 600 kΩ biasing resistances against ground

## FREQUENCY SELECTION

The frequency selection and power down control is accomplished via two digital control pins PDN1 and PDN2. The control logic is presented in table 1.

**Table 1** Frequency selection and power down control

PDN1	PDN2	RFI2 Switch	Selected Crystal Output	Description
High	High	Open	-	Power down
High	Low	Open	QO1	Frequency 1
Low	High	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna
Low	Low	Closed	QO2	Frequency 2, RFI2 capacitor connected in parallel with antenna

The internal antenna tuning capacitor switch (RFI2) and crystal filter output switches (QO1, QO2) are controlled according table 1. See switch in block diagram on page 1.

If frequency 1 is selected the RFI2 switch is open and only crystal output QO1 is active. Antenna frequency is determined by antenna inductor  $L_{ANT}$  (see Typical Application on page 5), antenna capacitor  $C_{ANT1}$  and parasitic capacitances related to antenna inputs RFI1, RFI2 and RFI3 (see Antenna Tuning Considerations below). Frequency 1 is the higher frequency of two selected frequencies.

If frequency 2 is selected then RFI2 switch is closed to connect  $C_{ANT2}$  in parallel with ferrite antenna and tune it to frequency 2. Then only crystal output QO2 is active. Frequency 2 is lower frequency of the two selected frequencies.

It is recommended to switch the device to power down for 50ms before switching to another frequency. This guarantees fast startup in switching to another frequency. The 50ms power down period is used to discharge AGC capacitor and to initialize fast startup conditions.

## ANTENNA TUNING CONSIDERATIONS

The ferrite bar antenna having inductance  $L_{ANT}$  and parasitic coil capacitance  $C_{COIL}$  is tuned to two reception frequencies  $f_1$  and  $f_2$  by parallel capacitors  $C_{ANT1}$  and  $C_{ANT2}$ . The receiver input stage and internal antenna capacitor switch have capacitances ( $C_{RFI1}$ ,  $C_{OFF2}$ ) which affect the resonance

frequencies.  $C_{OFF2}$  is switch capacitance when switch is open. When the switch is closed this capacitance is shorted by on resistance of the switch and is effectively eliminated. Following relationships can be written into two tuning frequencies.

Frequency  $f_1$  (higher frequency):

$$C_{TOT1} = C_{COIL} + C_{ANT1} + C_{RFI1} + C_{OFF2} = C_{COIL} + C_{ANT1} + 6.5\text{pF} + 37\text{pF} = C_{COIL} + C_{ANT1} + 43.5\text{pF}, \quad f_1 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT1}}}$$

Frequency  $f_2$  (lower frequency):

$$C_{TOT2} = C_{COIL} + C_{ANT1} + C_{ANT2} + C_{RFI1} = C_{COIL} + C_{ANT1} + C_{ANT2} + 6.5\text{pF}, \quad f_2 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT2}}}$$

## ABSOLUTE MAXIMUM RATINGS

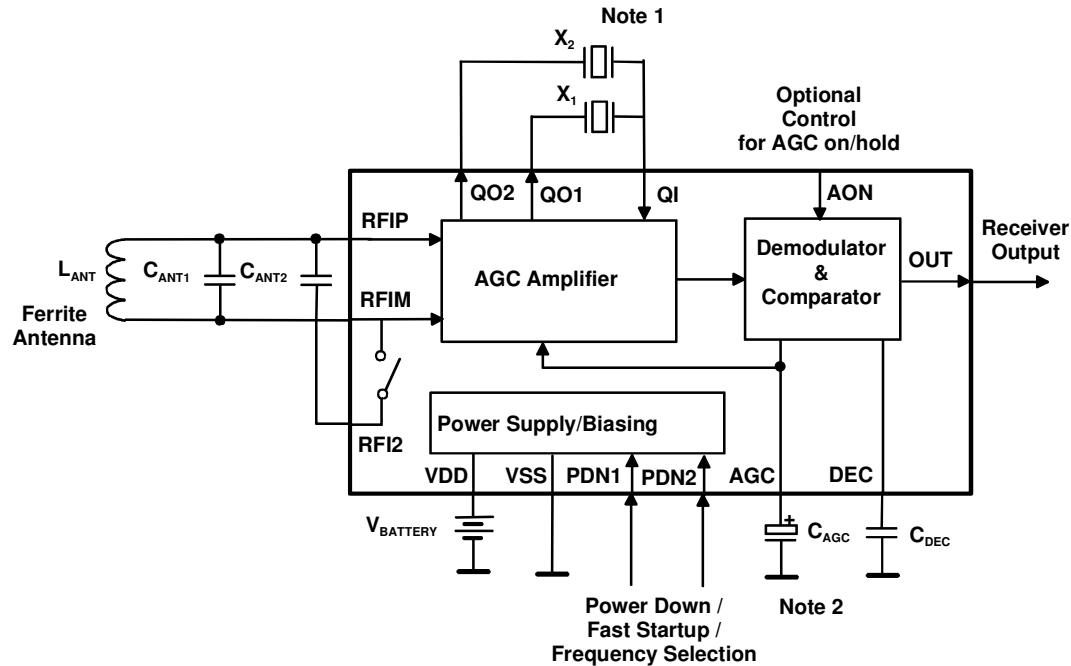
Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	$V_{DD}-V_{SS}$		-0.3	6	V
Input Voltage	$V_{IN}$		$V_{SS}-0.3$	$V_{DD}+0.3$	V
Power Dissipation	$P_{MAX}$			100	mW
Operating Temperature	$T_{OP}$		-40	+85	°C
Storage Temperature	$T_{ST}$		-55	+150	°C

## ELECTRICAL CHARACTERISTICS

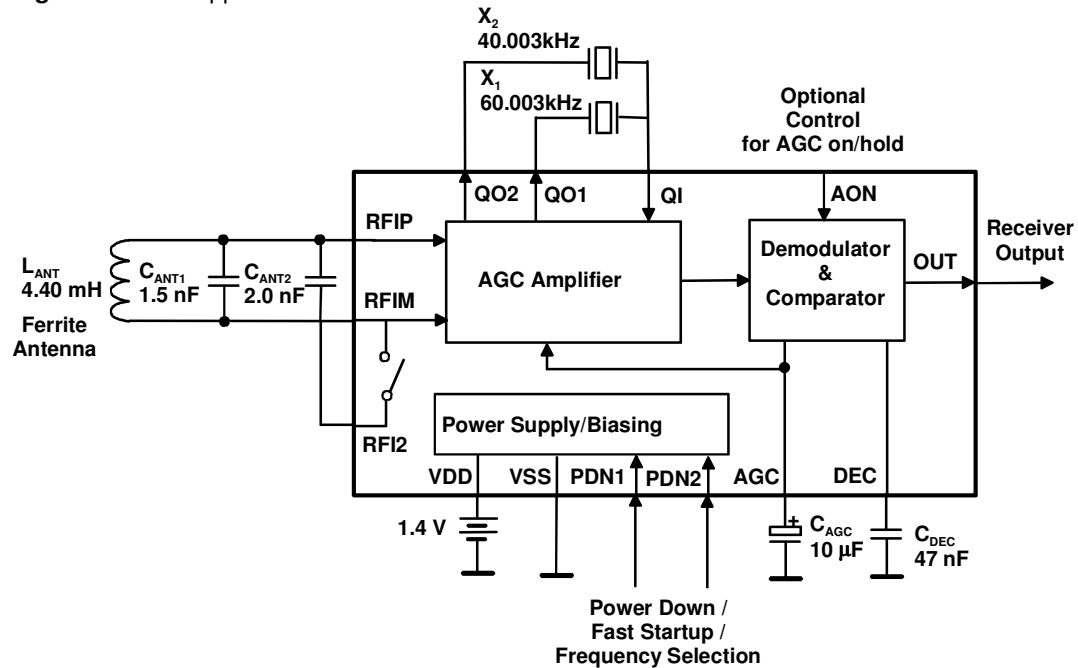
 Operating Conditions:  $V_{DD} = 1.4V$ , Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$		1.10		5	V
Current Consumption	$I_{DD}$	VDD=1.4 V, $V_{in}=0 \mu V_{rms}$ VDD=1.4 V, $V_{in}=20 mV_{rms}$ VDD=3.6 V, $V_{in}=0 \mu V_{rms}$ VDD=3.6 V, $V_{in}=20 mV_{rms}$	31	64 37 67 40	91 65	$\mu A$
Stand-By Current	$I_{DDoff}$				0.1	$\mu A$
Input Frequency Range	$f_{IN}$		40		100	kHz
Minimum Input Voltage	$V_{INmin}$			0.4	1	$\mu V_{rms}$
Maximum Input Voltage	$V_{INmax}$		20			mVrms
Receiver Input Resistance	$R_{RF1}$	$f=40kHz..77.5 kHz$		270		k $\Omega$
Receiver Input Capacitance	$C_{RF1}$			6.5		pF
RFI2 Switch On Resistance	$R_{ON2}$	VDD=1.4 V	10	3.8		$\Omega$
RFI2 Switch Off Resistance	$R_{OFF2}$			37		M $\Omega$
RFI2 Switch Off Capacitance	$C_{OFF2}$					pF
Input Levels $ I_{IN}  < 0.5 \mu A$	$V_{IL}$ $V_{IH}$		0.8 $V_{DD}$		0.2 $V_{DD}$	V
Output Current $V_{OL} < 0.2 V_{DD}; V_{OH} > 0.8 V_{DD}$	$ I_{OUT} $		5			$\mu A$
Output Pulse	$T_{100ms}$	$1 \mu V_{rms} \leq V_{IN} \leq 20 mV_{rms}$	50		140	ms
	$T_{200ms}$	$1 \mu V_{rms} \leq V_{IN} \leq 20 mV_{rms}$	150		230	ms
	$T_{500ms}$	$1 \mu V_{rms} \leq V_{IN} \leq 20 mV_{rms}$	400	500	600	ms
	$T_{800ms}$	$1 \mu V_{rms} \leq V_{IN} \leq 20 mV_{rms}$	700	800	900	ms
Startup Time	$T_{Start}$	Fast Start-up, $V_{in}=0.4 \mu V_{rms}$ Fast Start-up, $V_{in}=20 mV_{rms}$		1.3 3.5		s
Output Delay Time	$T_{Delay}$			50	100	ms

**TYPICAL APPLICATION**



**Figure 1** Application circuit of dual band receiver MAS9081



**Figure 2** Example circuit of dual band receiver MAS9081 for MSF/WWVB/JJY frequencies

## TYPICAL APPLICATION (Continued)

### Note 1: Crystals

The crystals as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 2). The crystal shunt capacitance  $C_0$  should be matched as well as possible with the internal shunt capacitance compensation capacitor  $C_C$  of MAS9081. See Compensation Capacitance Options on table 3.

**Table 2** Time-Signal System Frequencies

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
HGB	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

**Table 3** Compensation Capacitance Options

Device	$C_C$	Crystal Description
MAS9081A1	0.75 pF	For low $C_0$ crystal
MAS9081A3	1.25 pF	For high $C_0$ crystal
MAS9081A4	1.5 pF	For high $C_0$ crystal
MAS9081A5	3.875 pF	For any crystal (over compensated, requires external capacitors)

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1pF floating package shunt capacitance can have 0.85pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

Highest frequency crystal is connected to crystal output pin 1 (QO1). Lowest frequency crystal is connected to crystal output pin 2 (QO2). The other pin of both crystals is connected to common crystal input pin QI.

Table 4 below presents some crystal manufacturers having suitable crystals for timesignal receiver application.

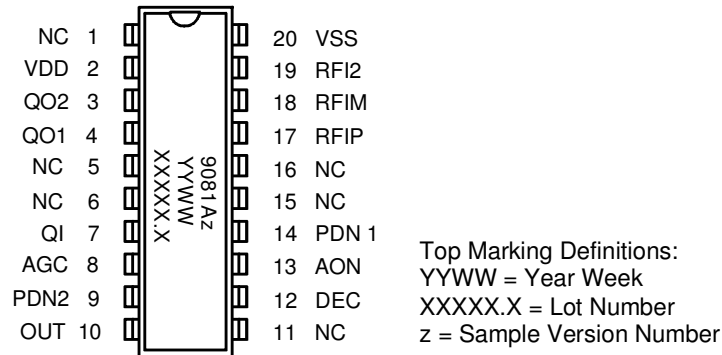
**Table 4.** Crystal Manufacturers and Crystal Types in Alphabetical Order for Timesignal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	<a href="http://www.citizen.co.jp/tokuhan/quartz/">http://www.citizen.co.jp/tokuhan/quartz/</a>
Epson	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	<a href="http://www.epsondevice.com/e/">http://www.epsondevice.com/e/</a>
KDS Daishinku	DT-261	ø 2.0 x 6.0	<a href="http://www.kdsj.co.jp/english.html">http://www.kdsj.co.jp/english.html</a>
Microcrystal	MX1V-L2N MX1V-T1K	ø 2.0 x 6.0 ø 2.0 x 8.1	<a href="http://www.microcrystal.com/">http://www.microcrystal.com/</a>
Seiko Instruments	VTC-120	ø 1.2 x 4.7	<a href="http://speed.sii.co.jp/pub/compo/quartz/topE.jsp">http://speed.sii.co.jp/pub/compo/quartz/topE.jsp</a>

### Note 2: AGC Capacitor

The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least several 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. DEC capacitor can be low leakage chip capacitor.

## MAS9081 SAMPLES IN SBDIL 20 PACKAGE



### PIN DESCRIPTION

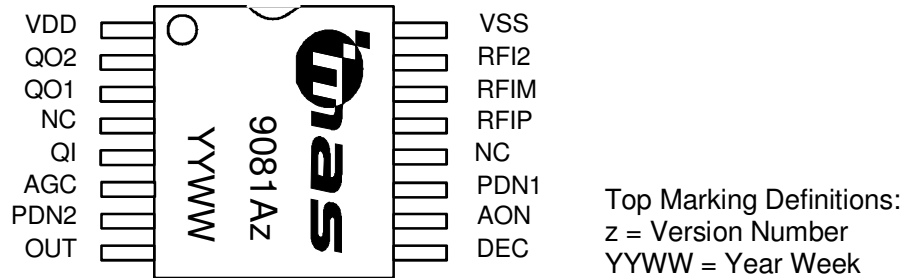
Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
QO2	3	AO	Quartz Filter Output for Crystal 2	
QO1	4	AO	Quartz Filter Output for Crystal 1	
NC	5			1
NC	6			1
QI	7	AI	Quartz Filter Input for Crystals	
AGC	8	AO	AGC Capacitor	
PDN2	9	DI	Power Down/Frequency Selection Input 2	
OUT	10	DO	Receiver Output	2
NC	11			
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	3
PDN1	14	DI	Power Down/Frequency Selection Input 1	
NC	15			
NC	16			
RFIP	17	AI	Positive Receiver Input	4
RFIM	18	AI	Negative Receiver Input	4
RFI2	19	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

#### Notes:

- Pins 5 and 6 between QO and QI must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- Receiver inputs RFIP and RFIM have both 600 k $\Omega$  biasing MOSFET-transistors towards ground

## PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



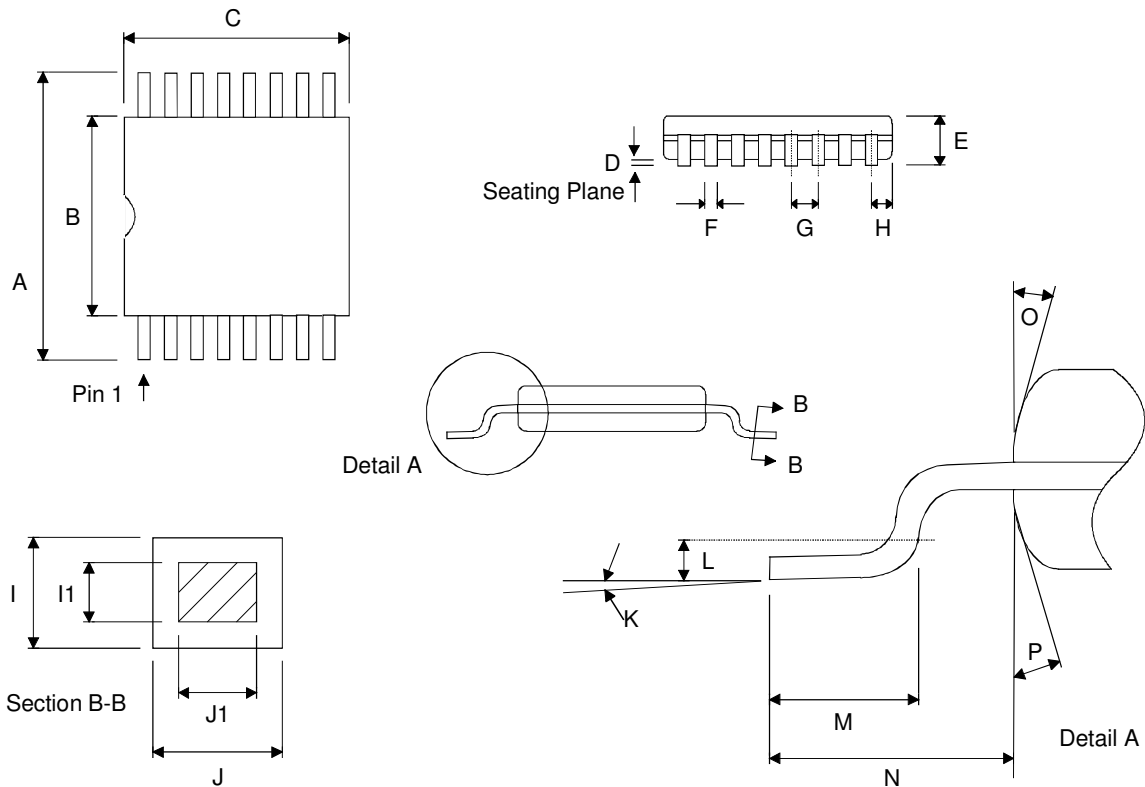
## PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
QO2	2	AO	Quartz Filter Output for Crystal 2	
QO1	3	AO	Quartz Filter Output for Crystal 1	
NC	4			1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	6	AO	AGC Capacitor	
PDN2	7	DI	Power Down/Frequency Selection Input 2	
OUT	8	DO	Receiver Output	2
DEC	9	AO	Demodulator Capacitor	
AON	10	DI	AGC On Control	3
PDN1	11	DI	Power Down/Frequency Selection Input 1	
NC	12			
RFIP	13	AI	Positive Receiver Input	4
RFIM	14	AI	Negative Receiver Input	4
RFI2	15	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	16	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

### Notes:

- Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up (to AGC on) with current  $< 1 \mu A$  which is switched off at power down
- Differential input versions A1..A5 have 600 k $\Omega$  biasing MOSFET-transistors towards ground from both receiver inputs RFIP and RFIM. Asymmetric input versions AB..AF have input pin RFIM unconnected.

**PACKAGE (TSSOP-16) OUTLINES**


Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M	0.50	0.75	mm
(The length of a terminal for soldering to a substrate)			
N	1.00 REF		mm
O	12°		
P	12°		

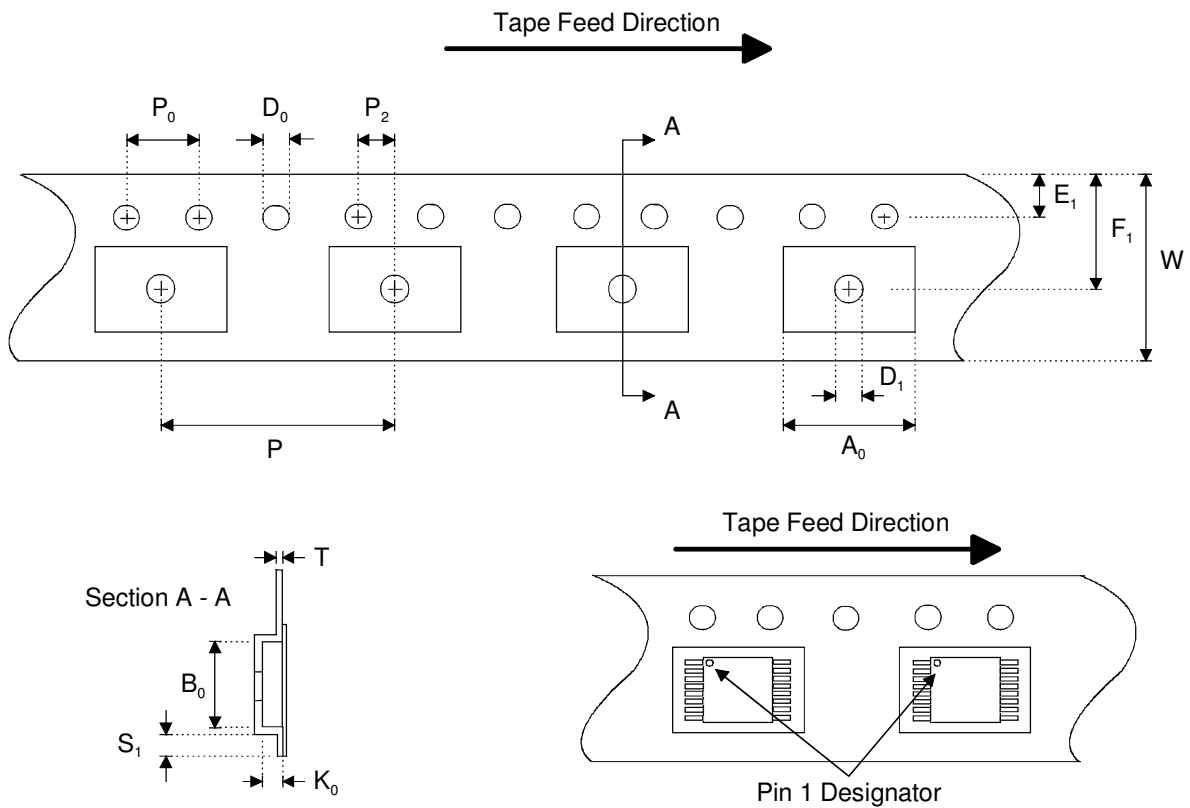
Dimensions do not include mold flash, protrusions, or gate burrs.  
 All dimensions are in accordance with JEDEC standard MO-153.

## SOLDERING INFORMATION

### ◆ For Pb-Free, RoHS Compliant TSSOP-16

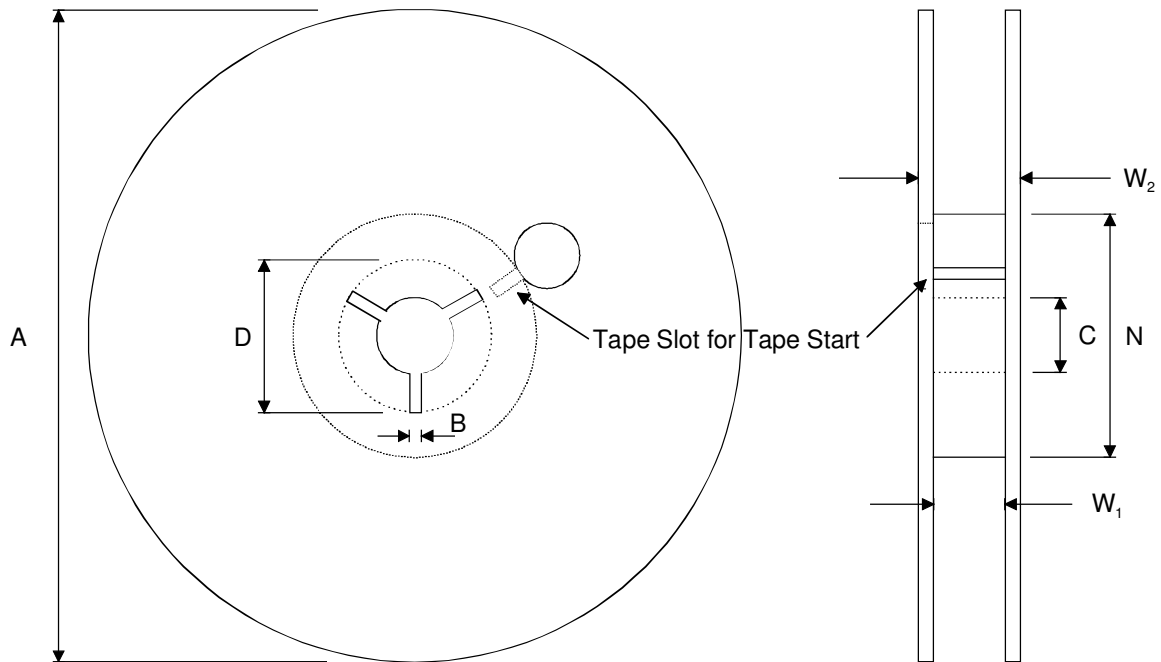
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. <a href="http://www.jedec.org">http://www.jedec.org</a>
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 μm, material Matte Tin

## EMBOSED TAPE SPECIFICATIONS



Dimension	Min	Max	Unit
A <sub>0</sub>	6.50	6.70	mm
B <sub>0</sub>	5.20	5.40	mm
D <sub>0</sub>	1.50 +0.10 / -0.00		mm
D <sub>1</sub>	1.50		mm
E <sub>1</sub>	1.65	1.85	mm
F <sub>1</sub>	7.20	7.30	mm
K <sub>0</sub>	1.20	1.40	mm
P	11.90	12.10	mm
P <sub>0</sub>	4.0		mm
P <sub>2</sub>	1.95	2.05	mm
S <sub>1</sub>	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

## REEL SPECIFICATIONS

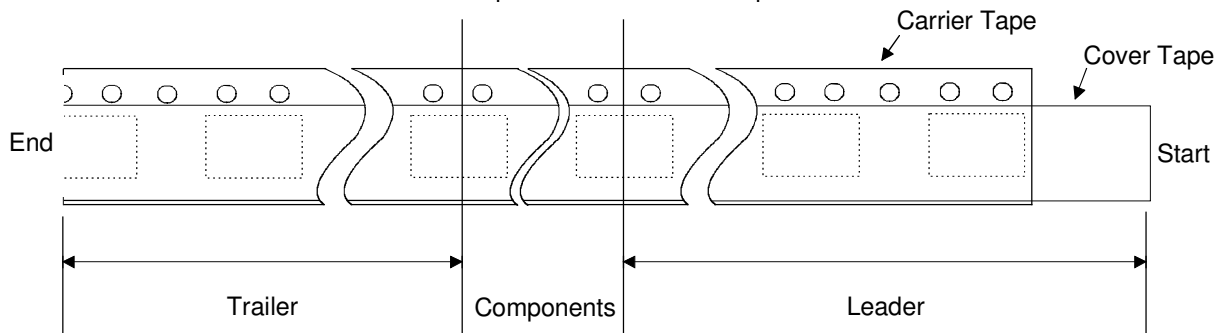


2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative

Carrier Tape Material: Conductive

Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
$W_1$ (measured at hub)	12.4	14.4	mm
$W_2$ (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

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## ORDERING INFORMATION

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Product Code	Product	Description	Capacitance Option
MAS9081A1TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 0.75 \text{ pF}$
MAS9081A3TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 1.25 \text{ pF}$
MAS9081A4TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 1.5 \text{ pF}$
MAS9081A5TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 $\mu\text{m}$ .	$C_C = 3.875 \text{ pF}$
MAS9081A1UC06	Dual Band AM-Receiver IC with Differential Input	TSSOP-16, Pb-free, RoHS compliant, Tape & Reel	$C_C = 0.75 \text{ pF}$

Contact Micro Analog Systems Oy for other wafer thickness options.

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## MICRO ANALOG SYSTEMS OY CONTACTS

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