

MAS6279**IC FOR 6.50 – 52.00 MHz VCTCXO****Preliminary**

- Fifth Order Compensation
- Frequency Stability ± 0.28 ppm
- Wide Range of Frequency
- Very Low Phase Noise
- Minimum Operating Temperature -40 °C
- PROM Selectable Output
- Tri State Output

DESCRIPTION

The MAS6279 is an integrated circuit well suited to build high end VCTCXO for telecommunication. The trimming is done through a serial bus and the calibration information is stored in an internal PROM. This means no rework for trimming is needed.

To build a VCTCXO only crystal is required in addition to MAS6279. The compensation method is fully analog, working continuously without generating any steps or other interference.

FEATURES

- Very small size
- Minimal current consumption
- Wide operating temperature range
- Very low phase noise
- Programmable VC-sensitivity
- Minimum operating temperature -40 °C
- Oscillator frequency output selectable by PROM direct or $f_0/2$.
- Output waveform selectable by PROM: sine wave or CMOS.
- MAS6279A2 version for external varactor
- Possibility to use just a compensation part

APPLICATIONS

- (VC)TCXO for high end telecommunications systems
- (VC)TCXO for GPS

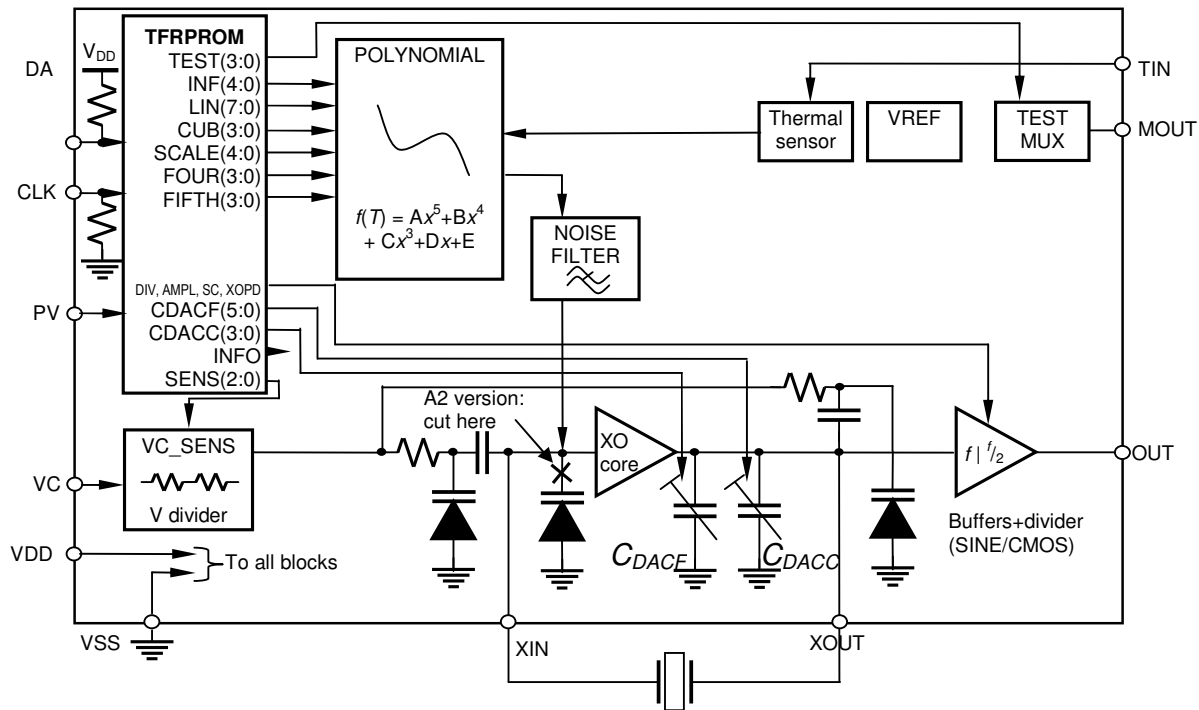
BLOCK DIAGRAM


Figure 1. Block diagram of MAS6279.

PIN DESCRIPTION

Pin Description	Symbol	x-coordinate	y-coordinate	Note
Power Supply Voltage	VDD	192	1364	
Programming Input	PV	710	1365	
Serial Bus Clock Input	CLK	1378	1364	
Serial Bus Data Input	DA	1609	1364	
Temperature Input / Output	TIN	2198	1355	
Voltage Control Input	VC	142	141	
XO Input (crystal connection)	XIN	606	141	
XO Output (crystal connection)	XOUT	1296	141	
Power Supply Ground	VSS	1801	141	
Buffered Output (frequency output)	OUT	1999	141	
Test Multiplexer Output	MOUT	2189	141	

Note: Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Pad coordinates are measured from the left bottom corner of the chip to the centres of the pads. The coordinates may vary depending on sawing width and location. However, the distances between the pads are accurate.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	$V_{DD} - V_{SS}$	-0.3	6.0	V	
Input Voltage	V_{IN}	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V	1)
Storage Temperature	T_{ST}	-55	150	°C	
Latchup Current Limit	I_{LUT}	±100		mA	

Note: Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

Note 1: Not valid for programming pin PV

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.6	2.8	5.3	V	
Operating Temperature	T_{OP}		-40		+85	°C	
Crystal Pulling Sensitivity	S		15	24	44	ppm/pF	
Crystal Load Capacitance	C_L	$VC = 1.3V$		8		pF	
Crystal R_s	R_s			20	50	Ω	

ELECTRICAL CHARACTERISTICS

(recommended operation conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note	
Crystal Frequency Range	f_c	13.00		52.00	MHz	1)	
Output Frequency Range	f_o	6.50		52.00	MHz	1)	
Voltage Control Range	VC	0	1.3	V_{DD}	V		
Voltage Control Sensitivity	VC_{SENS}		10		ppm/V	2)	
Frequency vs. Supply Voltage	df_o			± 0.2	ppm	3)	
Frequency vs. Load Change	df_o			± 0.2	ppm	4)	
Output voltage (10 k Ω 10 pF)	V_{out}	0.8	1.0		V _{pp}	5)	
Output voltage (10 k Ω 10 pF)	V_{out}			V_{DD}	V _{pp}	6)	
Rise and Fall Time (10 - 15 pF)			3		ns	6)	
Duty Cycle			40-60		%	6)	
Supply Current	I_{DD}		TBD		mA		
Compensation Range ± 1.0 ppm	T_C	-40		85	$^{\circ}C$		
Compensation Range ± 0.75 ppm	T_C	-20		70	$^{\circ}C$		
Compensation Range ± 0.28 ppm	T_C	10		50	$^{\circ}C$		
Compensation Range Linear Part	a_1	-0.4		-0.1	ppm/K		
Compensation Inflection Point	INF	23		31	$^{\circ}C$		
Compensation Range Cubic Part	a_3		95		ppm ² /K ³		
Amplitude Start up Time	T_{START}		2		ms		
Tri State Output Buffer OFF State ON State	DA	0 $V_{DD}-0.6$		0.55 V_{DD}	V		
Phase Noise	@ 1Hz			-60		dBc/Hz	7)
	@ 10Hz			-90			
	@ 100Hz			-113			
	@ 1kHz			-136			
	@ 10kHz			-148			
	@ 100kHz			-155			

Note 1: Frequency division by two is selected by PROM bit DIV: 0=no division, 1=div by 2
 Thus IC output frequency range is 6.5 MHz – 52 MHz.

Note 2: Depending on a crystal pulling.

Note 3: $V_{DD} \pm 5\%$

Note 4: $R_L = 10\text{ k}\Omega \pm 10\%$, In sine wave output $C_L = 10\text{ pF} \pm 10\%$, In CMOS output $C_L = 15\text{ pF} \pm 10\%$

Note 5: Output is selected by PROM bit AMPL: 0=0.8 V_{pp}, 1=1.0V_{pp}, sine mode only!

Note 6: CMOS output

Note 7: Not measured in production testing; guaranteed by design

IC OUTLINES



Figure 2. MAS6279

Note1: Die map reference is the actual left bottom corner of the sawn chip.

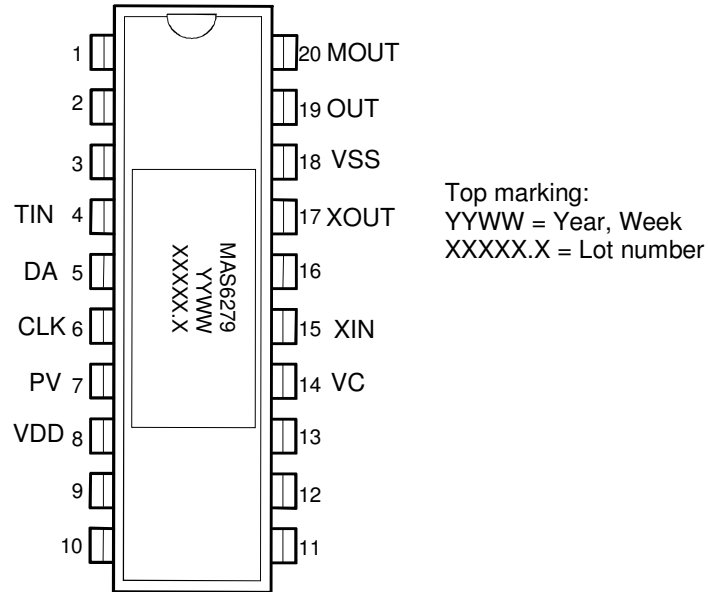
Note2: Pad size is 80 μm x 80 μm, except for pads VDD and VSS size is 180μm x 80μm.

Note3: See coordinates in pin description.

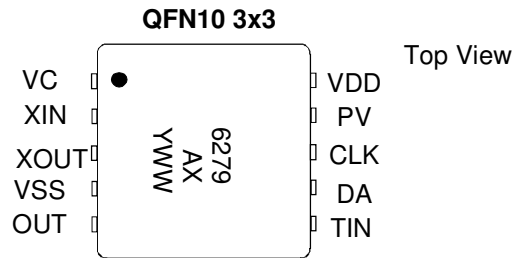
Note4: Die dimensions include 80 μm scribes for both sides. The actual dimensions are a bit less due to the saw width.

Note 5: Pins CLK and PV can either be connected to VSS or left floating, and pin TIN must be left floating in VCTCXO module end-user application. Pin DA has to be connected to VDD in normal operation.

SAMPLES IN SBDIL 20 PACKAGE

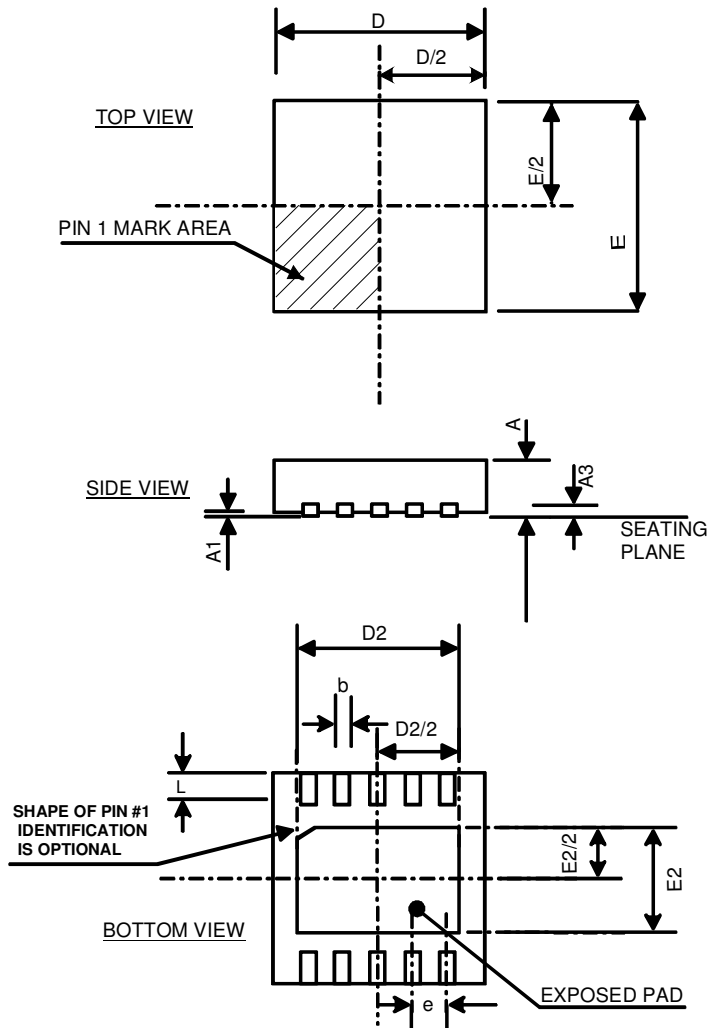


DEVICE OUTLINE CONFIGURATION



A = product version
X = Varactor type
Y = year
WW = week

PACKAGE (QFN 3X3x0.75 10ld) OUTLINE



Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.700	0.750	0.800	mm
A1	0.000	0.020	0.050	mm
A3	0.178	---	0.228	mm
b	0.200	---	0.300	mm
D	2.950	3.000	3.050	mm
D2 (Exposed.pad)	2.350	---	2.450	mm
E	2.950	3.000	3.050	mm
E2 (Exposed.pad)	1.650	---	1.750	mm
e	0.500 BSC			mm
L	0.350	---	0.450	mm

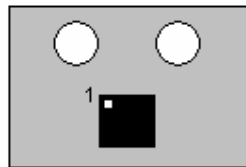
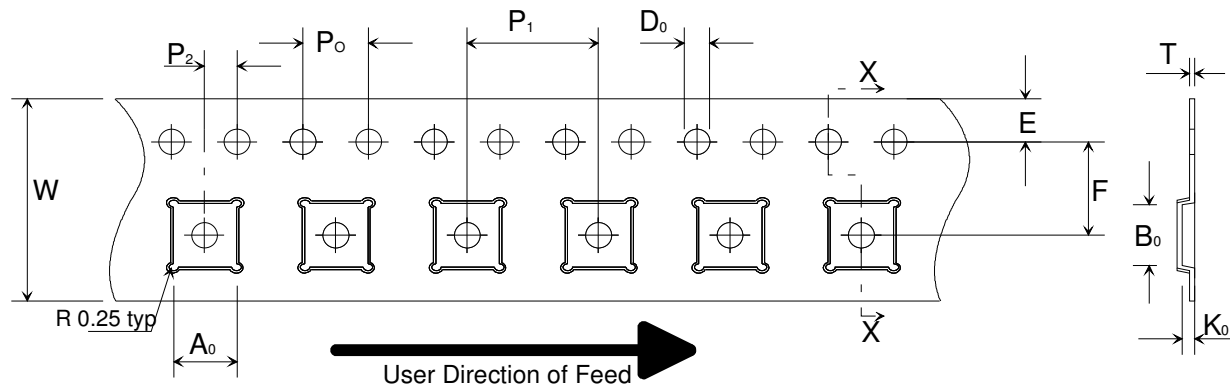
Dimensions do not include mold or interlead flash, protrusions or gate burrs.

SOLDERING INFORMATION

◆ For Lead-Free / Green QFN 3mm x 3mm x 0.75mm

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	7.62 - 25.4 μm, Matte Tin

EMBOSSED TAPE SPECIFICATIONS

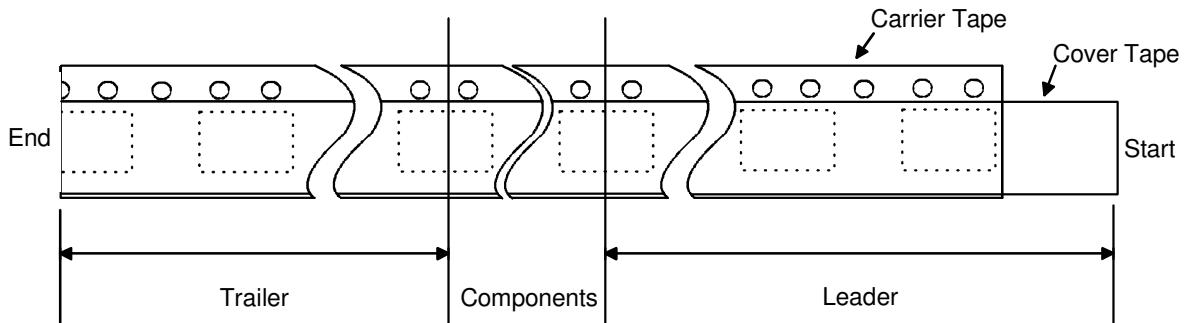
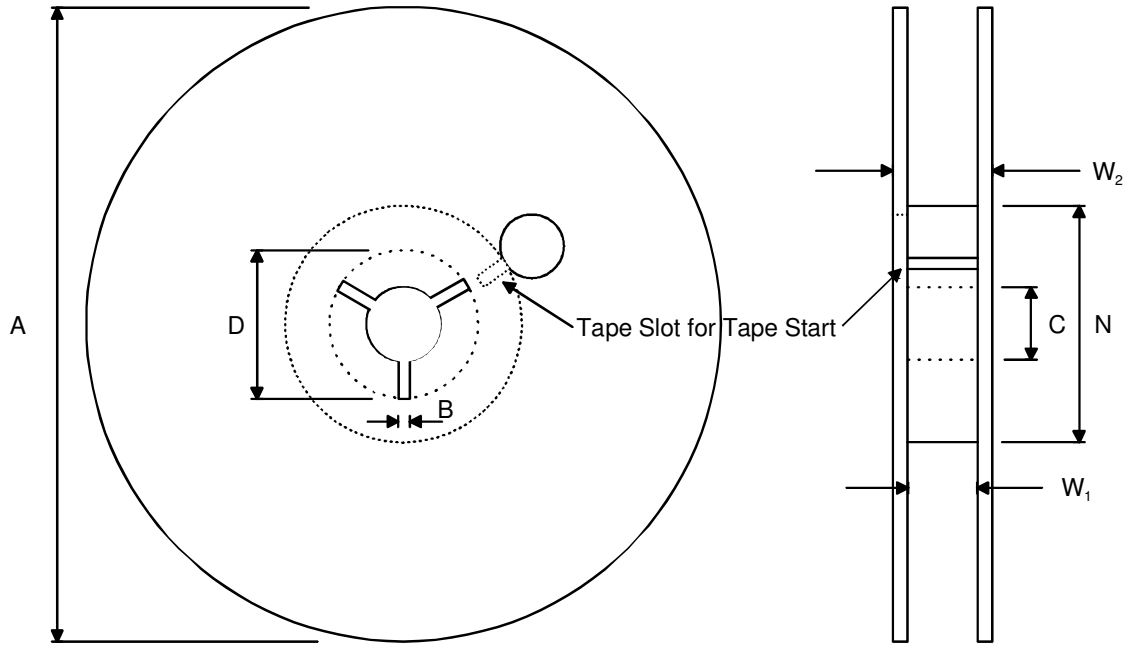


Orientation on tape

Dimension	Min/Max	Unit
A ₀	3.30 ±0.10	mm
B ₀	3.30 ±0.10	mm
D ₀	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
K ₀	1.10 ±0.10	mm
P ₀	4.0	mm
P ₁	8.0 ±0.10	mm
P ₂	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

All dimensions in millimeters

REEL SPECIFICATIONS



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	100		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

3000 Components on Each Reel
 Reel Material: Conductive, Plastic Antistatic or Static Dissipative
 Carrier Tape Material: Conductive
 Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS6279A1TG00	IC for VCTCXO	EWS Tested wafer 215 μ m	Integrated varactor
MAS6279A1HP06	IC for VCTCXO	QFN10, T&R 3000 pcs / r, Pb free RoHS	Integrated varactor
MAS6279A2TG00	IC for VCTCXO	EWS Tested wafer 215 μ m	External varactor
MAS6279A2HP06	IC for VCTCXO	QFN10, T&R 3000 pcs / r, Pb free RoHS	External varactor

Contact Micro Analog Systems Oy for other wafer thickness options.

◆ The formation of product code

Product name	Design version	Package type	Delivery format
MAS6279	A1 = Integrated varactor	TG = 215 μ m thick EWS tested wafer	00 = bare wafer
	A2 = External varactor	HP = QFN10 3x3x0.75 mm, Pb free, RoHS compliant	06 = tape & reel

LOCAL DISTRIBUTOR

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